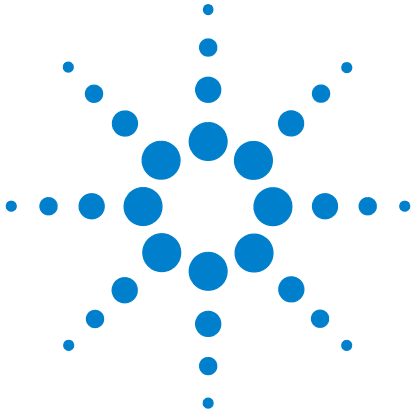

Agilent N5392A Ethernet Compliance Test Application

Methods of Implementation

Agilent Technologies

Notices

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Ethernet Automated Testing—At A Glance

The Agilent N5392A Ethernet Compliance Test Application helps you verify Ethernet transmitter device under test (DUT) compliance to specifications with the Agilent Infiniium digital storage oscilloscopes. The Ethernet Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE The tests performed by the Ethernet Compliance Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

Compliance testing measurements are described in the *IEEE 802.3- 2008 Standard* and the *ANSI X3.263- 1995 Standard*. For more information, see the IEEE 802 Standards web site at www.ieee802.org.

Required Equipment and Software

In order to run the Ethernet Compliance Test Application, you need the following equipment and software:

- N5392A Ethernet Compliance Test Application software.
- The minimum version of Infiniium oscilloscope software (see the N5392A test application release notes).
- Agilent N5395A and N5395B Ethernet electrical compliance test fixtures.
- InfiniiMax probe amplifiers.
- E2678A differential socket probe head.
- E2677A differential solder-in probe head.
- BNC cables.
- Keyboard, quantity = 1 (provided with Agilent Infiniium oscilloscope).
- Agilent also recommends using a second monitor to view the automated test application.
- Mouse, quantity = 1 (provided with Agilent Infiniium oscilloscope).

- For more details on the required and recommended equipments, please refer to “Required and Recommended Equipment" on page 18.

Below are the required licenses:

- N5392A Ethernet Compliance Test Application license.
- For jitter and distortion test, at least 8MPoints of memory is required. Hence, Memory Upgrade Option 001 is recommended for the 54850 and 80000 Series oscilloscopes for best performance. Option 080 is recommended for the 54830 and 8000 Series oscilloscopes.

In This Book

This manual describes the tests that are performed by the Ethernet Compliance Test Application in more detail; it contains information from (and refers to) the *IEEE 802.3- 2008 Standard* and the *ANSI X3.263- 1995 Standard*, and it describes how the tests are performed.

- Chapter 1, "Overview" describes the tests supported by the Ethernet Compliance Test Application and the standard references.
- Chapter 2, "Installing the Ethernet Compliance Test Application" shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 3, "Preparing to Take Measurements" shows how to start the Ethernet Compliance Test Application and gives a brief overview of how it is used.
- Chapter 4, "1000 Base-T Tests" contains more information on the 1000 Base-T tests.
- Chapter 5, "100 Base-TX Tests" contains more information on the 100 Base-TX tests.
- Chapter 6, "10 Base-T Tests" contains more information on the 10 Base-T tests.
- Appendix 7, "Calibrating the Infiniium Oscilloscope and Probe" describes how to calibrate the oscilloscope in preparation for running the Ethernet automated tests.
- Appendix 8, "InfiniiMax Probing" describes the InfiniiMax probe amplifiers and probe head recommendations for Ethernet testing.

See Also

- The Ethernet Compliance Test Application's online help, which describes:
  - Creating or opening a test project.
  - Setting up tests.
  - Selecting tests.
  - Configuring selected tests.
  - Connecting the oscilloscope to the DUT.
  - Running tests.
  - Viewing test results.
  - Viewing/printing the HTML test report.
  - Saving test projects.

Contents

4 1000 Base-T Tests

5 100 Base-TX Tests

1 Overview

The N5392A Ethernet Compliance Test Application performs the following tests as per the IEEE 802.3-2008 and ANSI X3.263-1995 standards.

Table 1 1000 Base-T Tests by Standard Reference

Standard Reference	Description	See
IEEE 802.3-2008 Sub clause 40.6.1.2.1	Output voltage	page 44
IEEE 802.3-2008 Sub clause 40.6.1.2.3	Template test	page 47
IEEE 802.3-2008 Sub clause 40.6.1.2.2	Droop test	page 49
IEEE 802.3-2008 Sub clause 40.6.1.2.4	Transmitter distortion test	page 58
IEEE 802.3-2008 Sub clause 40.6.1.2.5	Jitter master unfiltered	page 62
IEEE 802.3-2008 Sub clause 40.6.1.2.5	Jitter master filtered	page 66
IEEE 802.3-2008 Sub clause 40.6.1.2.5	Jitter slave unfiltered	page 70
IEEE 802.3-2008 Sub clause 40.6.1.2.5	Jitter slave filtered	page 75
IEEE 802.3-2008 Sub clause 40.8.3.3	MDI common mode output voltage	page 54
IEEE 802.3-2008 Sub clause 40.8.3.1	MDI return loss	page 91

Table 2 100 Base-TX Tests by Standard Reference

Standard Reference	Description	See
ANSI X3.263-1995, Section 9.1.2.2	UTP $+V_{out}$ differential output voltage	page 102
ANSI X3.263-1995, Section 9.1.2.2	UTP $-V_{out}$ differential output voltage	page 102
ANSI X3.263-1995, Section 9.1.4	Signal amplitude symmetry	page 103
ANSI X3.263-1995, Section 9.1.3	$+V_{out}$ overshoot	page 105
ANSI X3.263-1995, Section 9.1.3	$-V_{out}$ overshoot	page 105
ANSI X3.263-1995, Annex J	UTP AOI template	page 107
ANSI X3.263-1995, Section 9.1.8	Duty cycle distortion	page 114
ANSI X3.263-1995, Section 9.1.9	Transmit jitter	page 112
ANSI X3.263-1995, Section 9.1.6	AOI $+V_{out}$ rise time	page 109
ANSI X3.263-1995, Section 9.1.6	AOI $+V_{out}$ fall time	page 109
ANSI X3.263-1995, Section 9.1.6	AOI $+V_{out}$ rise/full-time symmetry	page 109
ANSI X3.263-1995, Section 9.1.6	AOI $-V_{out}$ rise time	page 109
ANSI X3.263-1995, Section 9.1.6	AOI $-V_{out}$ fall time	page 109
ANSI X3.263-1995, Section 9.1.6	AOI $-V_{out}$ rise/fall time symmetry	page 109
ANSI X3.263-1995, Section 9.1.5	Transmitter return loss	page 118
ANSI X3.263-1995, Section 9.2.2	Receiver return loss	page 123

Table 3 10 Base-T Tests by Standard Reference

Standard Reference	Description	See
IEEE 802.3-2008 Sub clause 14.3.1.2.1, Figure 14-12	Template Link Pulse with TPM	page 133
IEEE 802.3-2008 Sub clause 14.3.1.2.1, Figure 14-10	Template TP_IDL with TPM	page 137
IEEE 802.3-2008 Sub clause 14.3.1.2.1, Figure 14-9, Table 14-1	Template MAU	page 140
IEEE 802.3-2008 Sub clause 14.3.1.2.3 and Annex B.4.1 and B.4.3.3	Jitter with TPM	page 143
IEEE 802.3-2008 Sub clause 14.3.1.2.1, Figure 14-12	Template Link Pulse without TPM	page 148
IEEE 802.3-2008 Sub clause 14.3.1.2.1, Figure 14-10	Template TP_IDL without TPM	page 151
IEEE 802.3-2008 Sub clause 14.3.1.2.3 and Annex B.4.1 and B.4.3.3	Jitter without TPM	page 155
IEEE 802.3-2008 Sub clause 14.3.1.2.1	Peak differential output voltage	page 157
IEEE 802.3-2008 Sub clause 14.3.1.2.1	Harmonic content	page 159
IEEE 802.3-2008 Sub clause 14.3.1.2.5	Common mode output voltage	page 162
IEEE 802.3-2008 Sub clause 14.3.1.2.2 and Annex B.4.3.2	Transmitter return loss	page 168
IEEE 802.3-2008 Sub clause 14.3.1.3.4 and Annex B.4.3.5	Receiver return loss	page 173

1 Overview

2 Installing the Ethernet Compliance Test Application

If you purchased the N5392A Ethernet Compliance Test Application separately, you need to install the software and license key.

Installing the Software

1. Make sure you have the required version of the Infiniium oscilloscope software:
   a. See the compliance test application release notes for the required minimum version of the software.
   b. To check the software version on the oscilloscope, choose **Help>About Infiniium...** from the main menu.
2. To obtain the Ethernet Compliance Test Application, go to Agilent website: http://www.agilent.com/find/scope-apps-sw.

   The link for Ethernet Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

Installing the License Key

1. Request a license code from Agilent by following the instructions on the Entitlement Certificate.

   You will need the oscillocope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog.
2. After you receive your license code from Agilent, choose **Utilities>Install Option License...**.
3. In the Install Option License dialog, enter your license code and click **Install License**.

4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.

5 Click **Close** to close the Install Option License dialog.

6 Choose **File>Exit**.

7 Restart the Infiniium oscilloscope application software to complete the license installation.

3 Preparing to Take Measurements

Before running the Ethernet automated tests, you need to acquire the appropriate test fixtures, and you should calibrate the oscilloscope. After the oscilloscope has been calibrated, you are ready to start the Ethernet Compliance Test Application and perform the measurements.

Required and Recommended Equipment

Test Fixtures

N5395A and N5395B Ethernet Electrical Compliance Test Fixtures

To use the N5392A Ethernet electrical performance validation and compliance software, you also need the Agilent N5395A or the N5395B Ethernet electrical compliance test fixture, at least one InfiniiMax active differential probe (1131A, 1132A or 1134A) with E2678A socketed differential probe head, and a BNC cable (for 1000 Base-T and 10 Base-T measurements only).

Figure 1, Figure 2 and Figure 3 show the N5395A and N5395B Ethernet electrical compliance test boards.

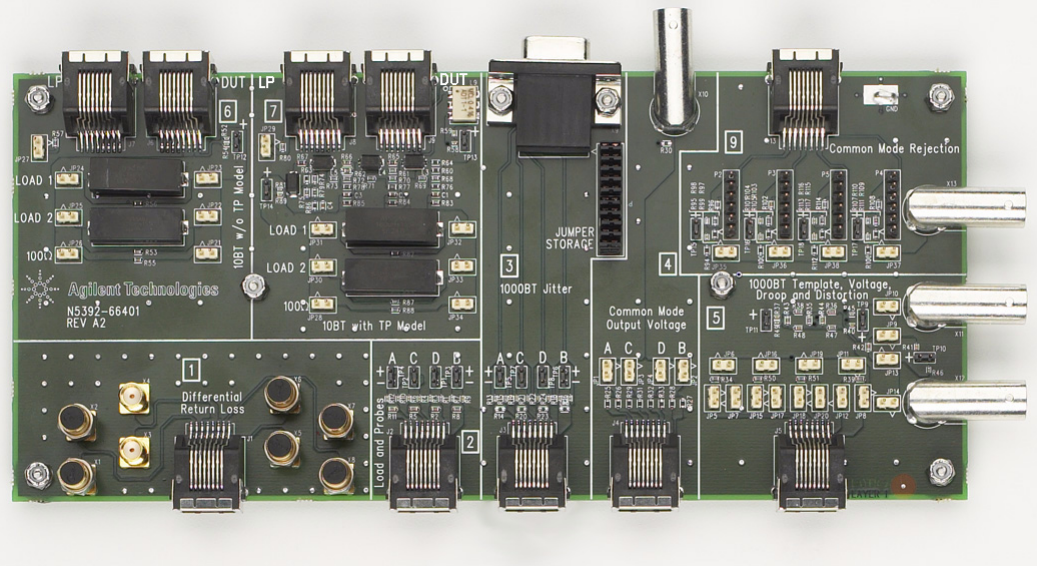


Figure 1 N5395A Ethernet Electrical Compliance Test Board - N5392-66401

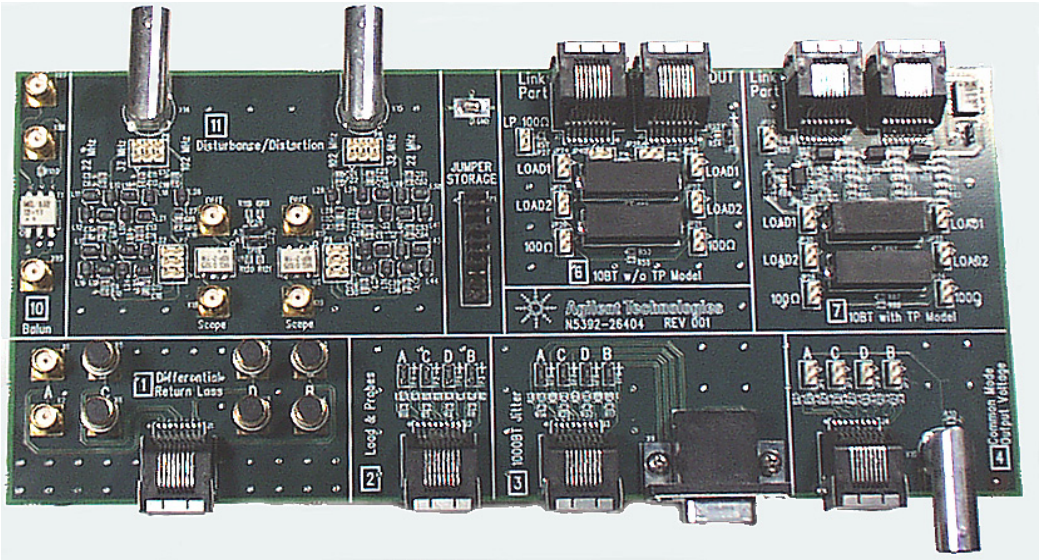


Figure 2 N5395B Ethernet Electrical Compliance Test Board - N5392-66404

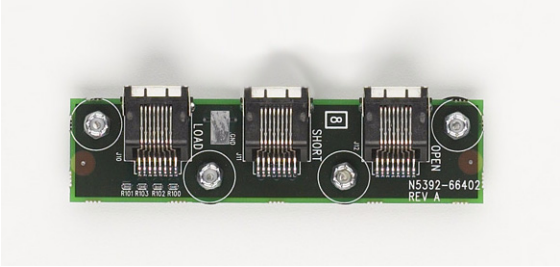


Figure 3 N5395A Ethernet Electrical Compliance Test Board - N5392-66402

Table 4 and Table 5 show the components of N5395A and N5395B Ethernet electrical compliance test boards.

Table 4 Components of N5395A Ethernet Electrical Compliance Test Board

Probes and BNC Cables	1000 Base-T Measurements
N5392-61601	Short RJ-45 cable for the Ethernet test application
N5392-66402	Return loss calibration test fixture
N5392-66401	Test fixture for the N5392A Ethernet test application

Table 5 Components of N5395B Ethernet Electrical Compliance Test Board

Probes and BNC Cables	1000 Base-T Measurements
N5392-61601	Short RJ-45 cable for the Ethernet test application
N5392-66403	Return loss calibration test fixture
N5392-66404	Test fixture for the N5392A Ethernet test application

Most of the compliance tests can use either board except for the 1000 Base-T distortion and return loss tests which require the N5395B board.

The Agilent Ethernet electrical compliance test fixture includes a main test fixture board, a short RJ-45 interconnect cable, and a small impedance calibration board. Probing points on the main test fixture board allow most oscilloscope measurements to be made using an Agilent InfiniiMax differential probe (1131A, 1132A, 1134A, 1168A, or 1169A) with an E2678A socketed differential probe head. Some measurements are made using a BNC cable. The 1000 Base-T jitter measurements are best made using two Agilent InfiniiMax active differential probes with E2677A solder-in differential probe heads.

Tests Supported by the N5395A Ethernet Test Fixture

The N5395A Ethernet electrical compliance test fixture provides some testing capability that is currently not automated by the N5392A Ethernet electrical performance validation and compliance software. Some of these tests require other equipment. The following tables list the tests supported by each section of the test fixture, the tests that are automated/supported by the N5392A software, and other hardware requirements.

- AWG = Arbitrary Waveform Generator required.
- VNA = Vector Network Analyzer required.
- LP = Link Partner Required.

Table 6 1000 Base-T Tests Supported by the N5395A Ethernet Test Fixture

Test Name	Ethernet Test Fixture Section									Jitter Test Cable	Supported by N5392A	LP	AWG	VNA
	1	2	3	4	5	6	7	8	9					
Template, Voltage, Droop (w/o Disturber)		X									X			
Jitter MASTER/SLAVE Unfiltered (w/ TX_TCLK)			X							X	X	X		
Jitter MASTER/SLAVE Unfiltered (w/o TX_TCLK)	X										X			
MASTER/ SLAVE JTxOut		X									X			
Jitter MASTER/ SLAVE Filtered (w/ TX_TCLK)		X[1]	X							X	X	X		
Jitter MASTER/ SLAVE Filtered (w/o TX_TCLK)	X										X			
Common Mode Output Voltage				X							X			
Distortion (w/o Disturber)		X												
Return Loss	X							X						X

[1] Jitter MASTER/SLAVE Filtered (w/ TX_TCLK) measurements require the JtxOut Measurement, which uses Fixture 2.

Table 7 100 Base-TX Tests Supported by the N5395A Ethernet Test Fixture

Test Name	Ethernet Test Fixture Section									Supported by N5392A	LP	VNA
	1	2	3	4	5	6	7	8	9			
Peak Voltage		X				X[2]				X	[2]	
Overshoot		X				X[2]				X	[2]	
Template		X				X[2]				X	[2]	
Jitter		X				X[2]				X	[2]	
Duty Cycle Distortion		X				X[2]				X	[2]	
Rise/Fall time Rise/Fall Symmetry		X				X[2]				X	[2]	
Return Loss	X							X				X

[2] A link partner MAY be required in order to obtain the 100BASE-TX test signal. These tests use fixture 6 when a link partner is required. Use fixture 2 if the device will output the test signal without connecting the DUT to a link partner.

Table 8 10 Base-T Tests Supported by the N5395A Ethernet Test Fixture

Test Name	Ethernet Test Fixture Section									Supported by N5392A	LP	VNA
	1	2	3	4	5	6	7	8	9			
Differential Output Voltage						X				X		
MAU Template							X			X		
TP_IDL/Link Pulse Template w/ TPM							X			X		
TP_IDL/Link Pulse Template w/o TPM						X				X		
Jitter, w/ TPM							X			X		
Jitter, w/o TPM						X				X		
Harmonic Content						X				X		
Common Mode Output Voltage				X						X		
Common Mode Rejection									X			
Return Loss	X							X				X

Tests Supported by the N5395B Ethernet Test Fixture

The N5395B Ethernet electrical compliance test fixture provides some testing capability that is currently not automated by the N5392A Ethernet electrical performance validation and compliance software. Some of these tests require other equipment. The following tables list the tests supported by each section of the test fixture, the tests that are automated/supported by the N5392A software, and other hardware requirements.

- AWG = Arbitrary Waveform Generator required.
- VNA = Vector Network Analyzer required.
- LP = Link Partner Required.

Table 9 1000 Base-T Tests Supported by the N5395B Ethernet Test Fixture

Test Name	Ethernet Test Fixture Section								Jitter Test Cable	Supported by N5392A	LP	AWG	VNA
	1	2	3	4	6	7	10	11					
Template, Voltage, Droop (w/ Disturber)	X							X		X		X	
Template, Voltage, Droop (w/o Disturber)		X								X			
Jitter MASTER/SLAVE Unfiltered (w/ TX_TCLK)			X						X	X	X		
Jitter MASTER/SLAVE Unfiltered (w/o TX_TCLK)	X									X			
MASTER/ SLAVE JTxOut		X								X			
Jitter MASTER/ SLAVE Filtered (w/ TX_TCLK)		X[1]	X						X	X	X		
Jitter MASTER/ SLAVE Filtered (w/o TX_TCLK)	X									X			
Common Mode Output Voltage				X						X			
Distortion (w/ Disturber)	1							X		X		X	
Distortion (w/o Disturber)		X								X			
Return Loss	X						X			X			X

[1] Jitter MASTER/SLAVE Filtered (w/ TX_TCLK) measurements require the JtxOut Measurement, which uses Fixture 2.

Table 10 100 Base-TX Tests Supported by the N5395B Ethernet Test Fixture

Test Name	Ethernet Test Fixture Section								Supported by N5392A	LP	VNA
	1	2	3	4	6	7	10	11			
Peak Voltage		X			X[2]				X	[2]	
Overshoot		X			X[2]				X	[2]	
Template		X			X[2]				X	[2]	
Jitter		X			X[2]				X	[2]	
Duty Cycle Distortion		X			X[2]				X	[2]	
Rise/Fall time Rise/Fall Symmetry		X			X[2]				X	[2]	
Return Loss	X						X		X		X

[2] A link partner MAY be required in order to obtain the 100BASE-TX test signal. Use fixture 6 when your device requires a link partner to output the test signal. Use fixture 2 when your device does not require a link partner to output the test signal.

Table 11 10 Base-T Tests Supported by the N5395B Ethernet Test Fixture

Test Name	Ethernet Test Fixture Section								Supported by N5392A	LP	VNA
	1	2	3	4	6	7	10	11			
Differential Output Voltage					X				X		
MAU Template						X			X		
TP_IDL/Link Pulse Template w/ TPM						X			X		
TP_IDL/Link Pulse Template w/o TPM					X				X		
Jitter, w/ TPM						X			X		
Jitter, w/o TPM					X				X		
Harmonic Content					X				X		
Common Mode Output Voltage				X					X		
Common Mode Rejection								X			
Return Loss	X						X				X

N5396A Gigabit Ethernet Jitter Test Cable

To make jitter measurements for 1000 Base-T, you need to use the N5396A Gigabit Ethernet jitter test cable along with the Ethernet test fixture, a second InfiniiMax active differential probe, and two E2677A solder-in differential probe heads.

The N5396A Gigabit Ethernet jitter test cable allows you to make 1000 Base-T jitter measurements with the Ethernet electrical compliance test fixture. The 103-m cable has a RJ-45 connector on one end to connect to a Link Partner, and a DB9 connector on the other end to connect to the Ethernet test fixture board.

Oscilloscope Compatibility and Recommended Probe Amplifiers

Table 12 Recommended Oscilloscopes and Recommended Probe Amplifiers

Standard	Data Rate	Recommended Oscilloscope	Oscilloscope Bandwidth	Recommended Probe	Probe Bandwidth
10 Base-T	10 Mb/s	Infiniium	≥ 600 MHz	113xA Series	≥ 3.5 GHz
100 Base-TX	100 Mb/s	Infiniium	≥ 600 Mhz	113xA Series	≥ 3.5 GHz
1000 Base-T	Gigabit Ethernet (4x250 Mb/s)	Infiniium	≥ 1 GHz	113xA Series	≥ 3.5 GHz

Number of Probes and BNC Cables Required

Table 13 Number of Probes and BNC Cables Required

Probes and BNC Cables	1000 Base-T Measurements	100 Base-TX Measurements	10 Base-T Measurements
InfiniiMax active differential probe	2	1	1
E2677A solder-in differential probe head	2		
E2678A socketed differential probe head	1	1	1
BNC cable	4		1

Supported Vector Network Analyzers for Return Loss Tests

- 8752x/3x Models
- 4395x/6x Models
- E5070x/71x Models
- E5061x/62x Models
- N5230A Model

Note: Before using the Vector Network Analyzers (VNA), it has to be calibrated and configured. The VNA should support a minimum of 1 MHz usable power range. For more details on VNA calibration, please refer to these chapters: “MDI Return Loss,” starting on page 91, “Transmitter Return Loss,” starting on page 118, “Receiver Return Loss,” starting on page 123, “Transmitter Return Loss,” starting on page 168 and “Receiver Return Loss,” starting on page 173.

Recommended Accessories

Table 14 Recommended Test Accessories

Agilent Part Number	Description
8120-1839	BNC cable (61 cm, 2 ft.)
8120-4948	SMA cable (90 cm, 3 ft.)
82357A/B	USB to GPIB Convertor
33250A	Function/Arbitrary Waveform Generator, Qty2
Not available	Optional push on SMA connectors for most efficient connection. Order 33SMA-Q50-0-4 from S.M. Electronics, Qty 6.

Recommended Infiniium Oscilloscope for Jitter and Distortion Test

For jitter and distortion test, it is recommended to have at least 8M Points of memory. Hence, option 001 is recommended for the 54850 and 80000 Series oscilloscopes for best performance. Option 080 is recommended for the 54830 and 8000 Series oscilloscopes.

Required Software

The minimum version of Infiniium oscilloscope software (see the N5392A test application release notes).

Calibrating the Oscilloscope

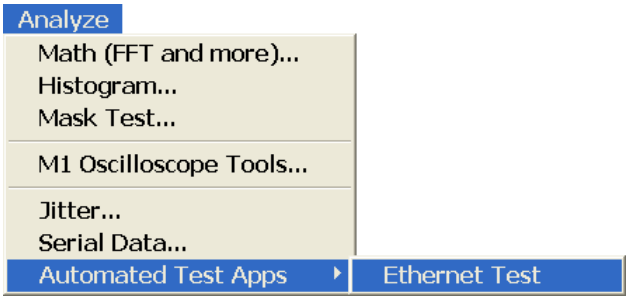
If you haven't already calibrated the oscilloscope, see Appendix 7, "Calibrating the Infiniium Oscilloscope and Probe".

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables or probes between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel for which they were calibrated.

Starting the Ethernet Compliance Test Application

1 From the Infiniium oscilloscope's main menu, choose Analyze>Automated Test Apps>Ethernet Test.



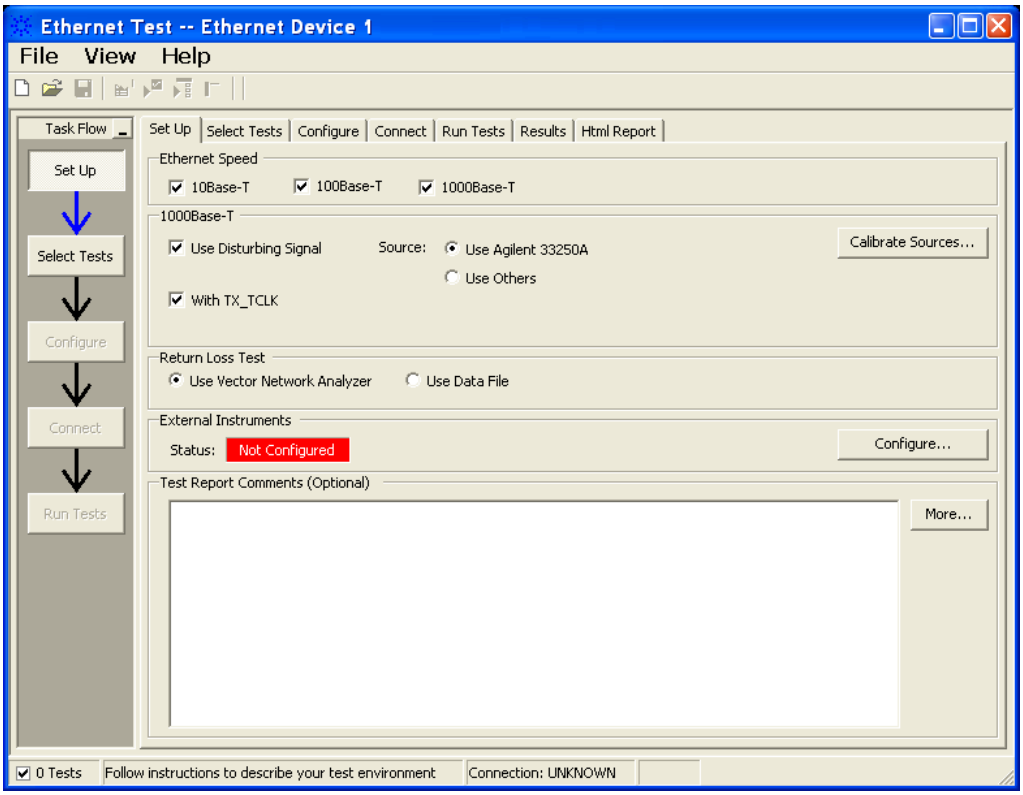


Figure 4 The Ethernet Compliance Test Application

NOTE If Ethernet does not appear in the Automated Test Apps menu, the Ethernet Compliance Test Application has not been installed (see Chapter 2, "Installing the Ethernet Compliance Test Application").

Figure 4 shows the Ethernet Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you select the Ethernet standards being tested. Lets you select whether or not a disturbing signal is used for testing 1000 Base-T. Lets you configure and calibrate external equipment. Lets you select the type of return loss test to run.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you enter information about the device being tested and configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

Online Help Topics

For information on using the Ethernet Compliance Test Application, see its online help (which you can access by choosing Help>Contents... from the application's main menu).

The Ethernet Compliance Test Application's online help describes:

- Creating or opening a test project.
- Setting up tests and equipment.
- Selecting tests.
- Configuring selected tests.
- Connecting the oscilloscope to the DUT.
- Running tests.
- Viewing test results.
- Viewing/exporting/printing the HTML test report.
- Saving test projects.
- User-defined add-ins.
- Controlling the application via a remote PC.
- Using a second monitor.

4
1000 Base-T Tests

This section provides the Methods of Implementation (MOIs) for 1000 Base-T tests using an Infiniium oscilloscope, InfiniiMax probes, and the Ethernet Compliance Test Application.

Probing for Test Mode 1 and Test Mode 4

Without Disturbing Signal Probing for Test Mode 1 and Test Mode 4

When performing 1000 Base-T Mode 1 tests, the Ethernet Compliance Test Application will prompt you to make the proper connections (also shown in Figure 5).

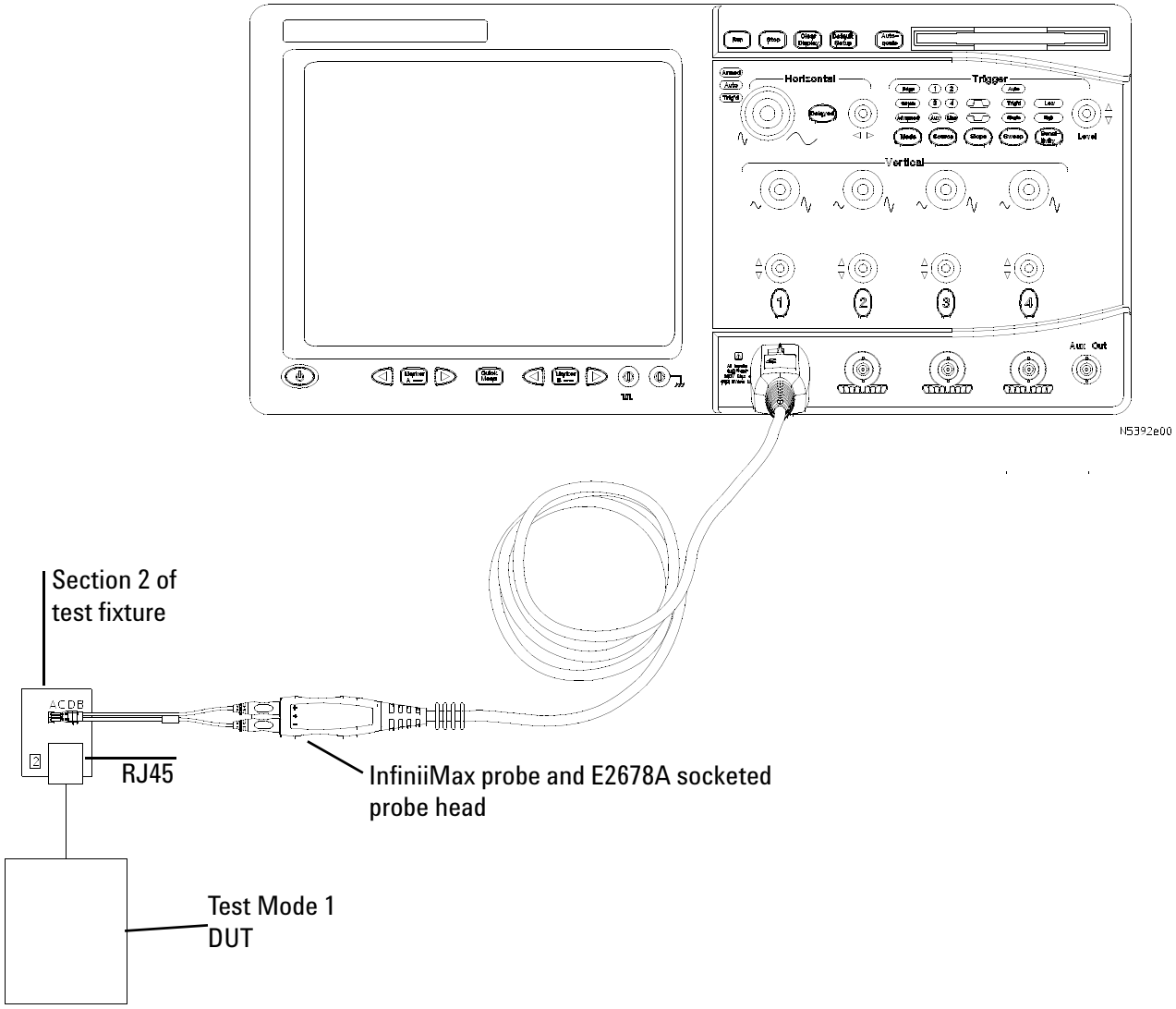


Figure 5 Probing for 1000 Base-T Test Mode 1 Tests

1 Connect the DUT to the RJ45 connector on section 2 of the Ethernet test fixture using a short straight-through UTP cable.

2 Connect an InfiniiMax probe with the E2678A socketed probe head to the test point for the pair you are testing (A, B, C, or D), and to the

oscilloscope channel which is selected as the “DUT Data” channel in the user interface’s “Configure” tab.

3 Ensure correct polarity of the probe head.

4 Ensure that the DUT is transmitting the appropriate “Test Mode 1” signal as indicated in the user interface.

You can use any oscilloscope channel for the DUT Data probe connection. You identify the channel used for DUT Data in the “Configure” tab of the Ethernet Compliance Test Application. (The channel shown in Figure 5 is just an example.)

For more information on the InfiniiMax probe amplifiers and differential probe heads, see Appendix 8, “InfiniiMax Probing,” starting on page 189.

Calibration Setup for the 33250A Disturbing Signal Source

Before running disturbing signal tests, the 33250A generators need to be calibrated. Connect the equipment as shown in Figure 6, “Calibration Setup for the 33250A Disturbing Signal Source,” on page 36 and Figure 7, “Rear Panel Cable Connections for the 33250A Generators,” on page 37.

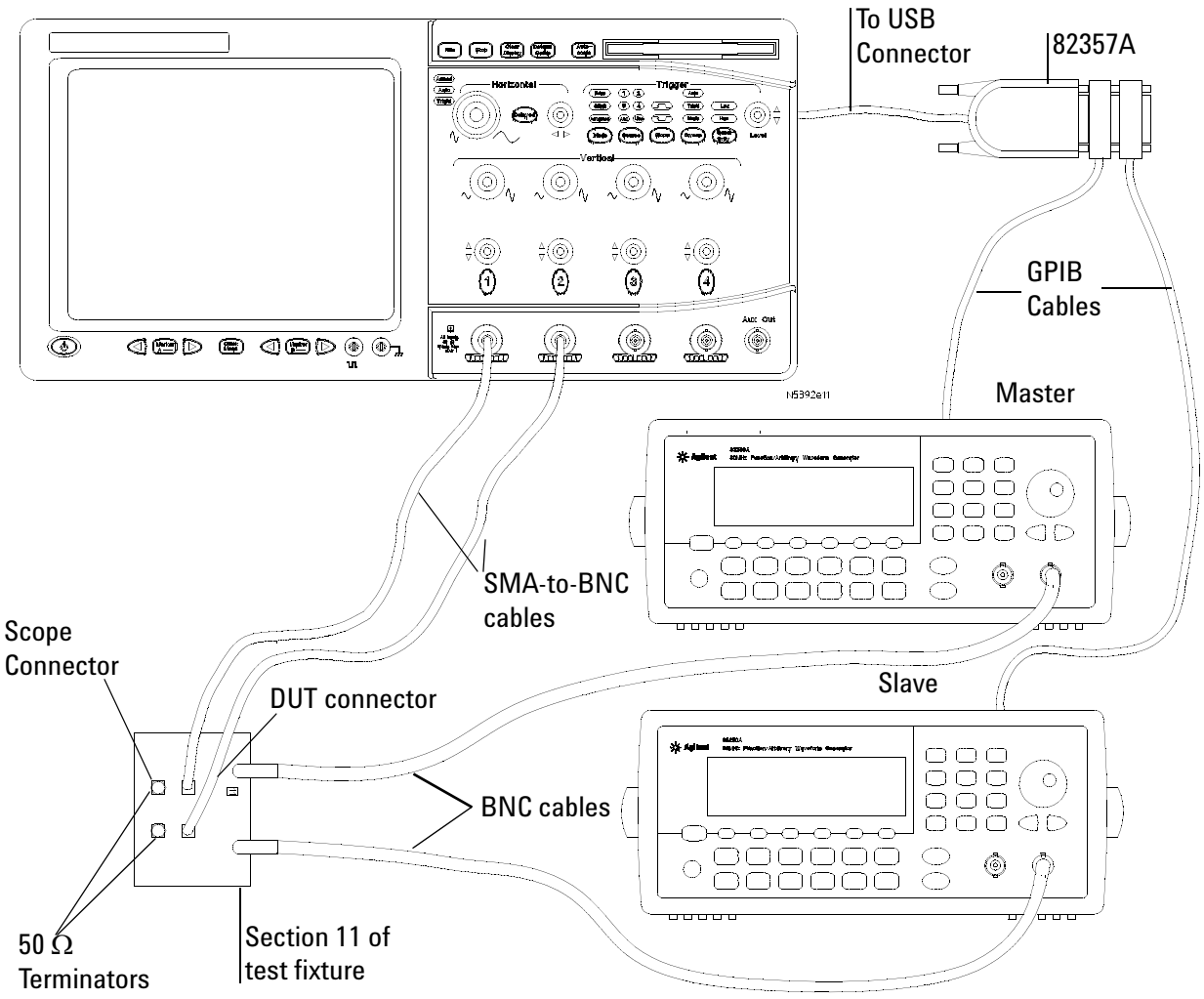


Figure 6 Calibration Setup for the 33250A Disturbing Signal Source

33250A Generator Setup

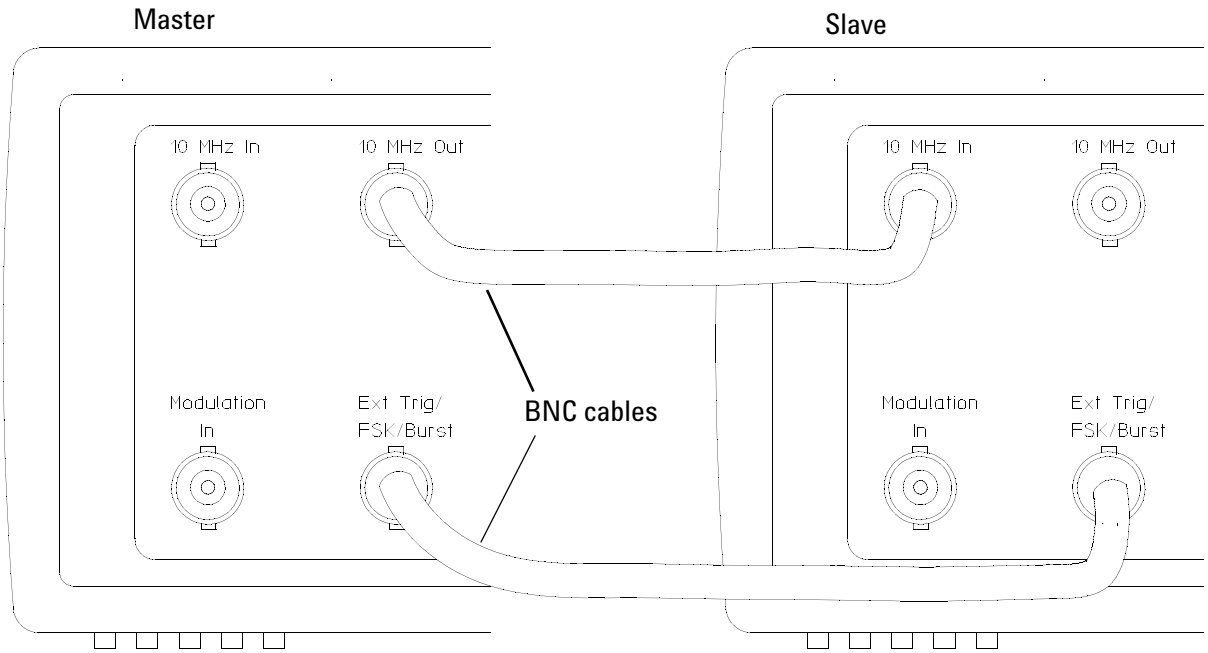


Figure 7 Rear Panel Cable Connections for the 33250A Generators

Performing the Calibration

1. Select the “Set Up" tab.
2. Select the "Calibrate Sources" button to start calibration process.
3. If the system is not physically configured to perform the calibration, the application will prompt you to change the physical configuration.

Disturbing Signal Probing Setup for Test Mode 1 and Test Mode 4 Using the 33250A Signal Generators

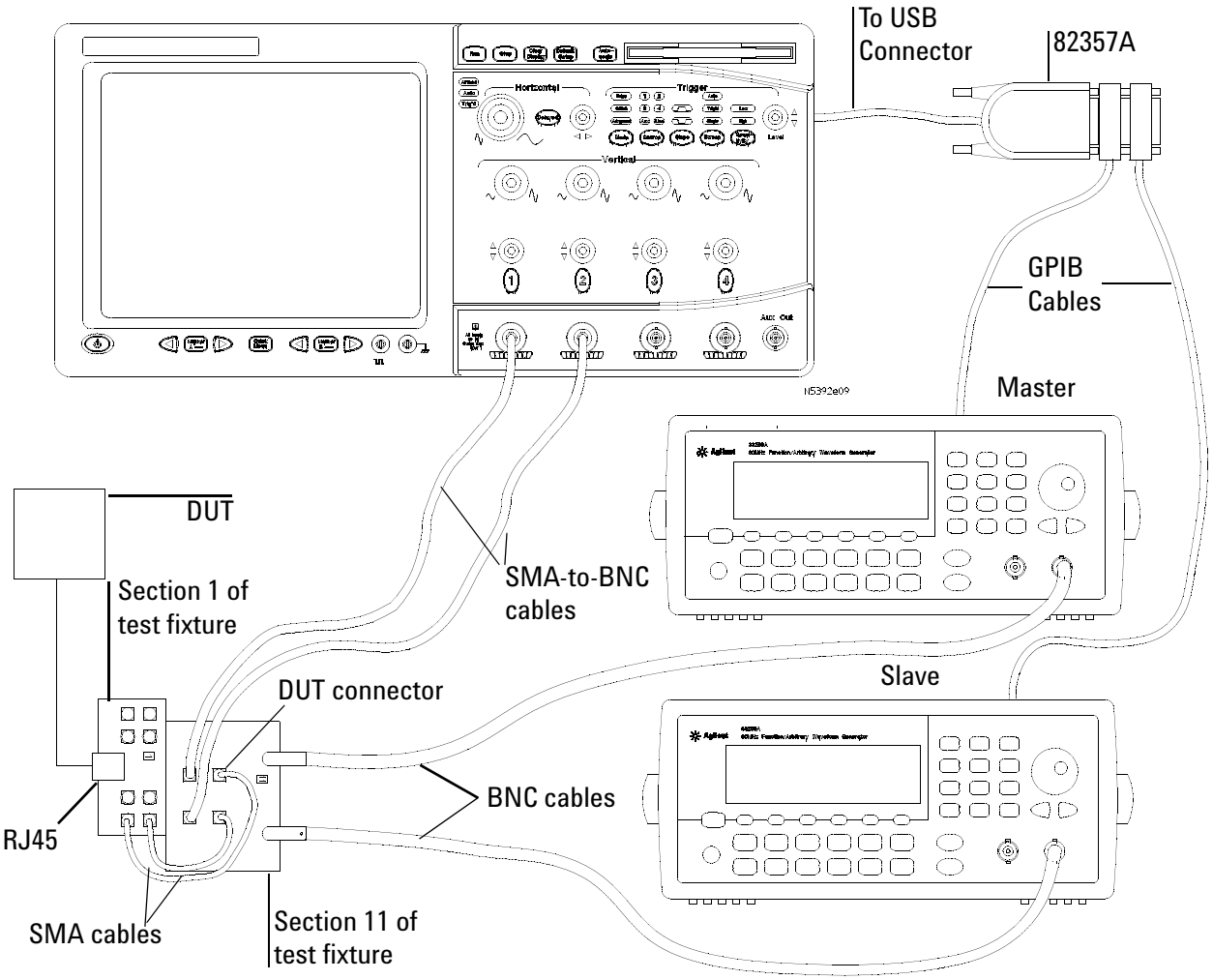


Figure 8 Probing and Cable Connections for Test Mode 1 and Test Mode 4 Using the 33250A Signal Generators

33250A Generator Setup

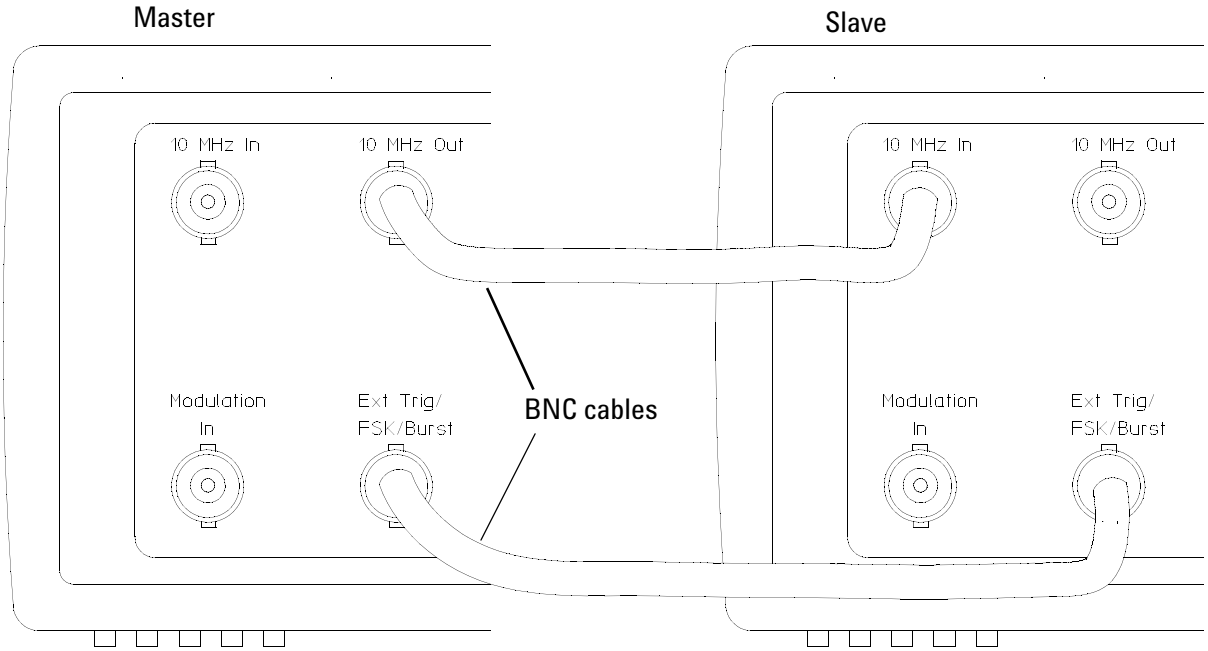
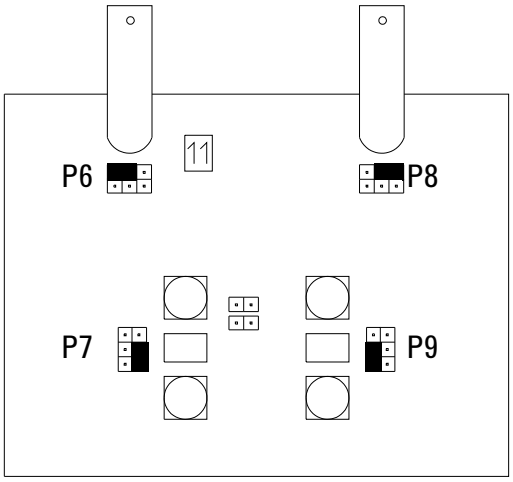


Figure 9 Rear Panel Cable Connections for the 33250A Generators

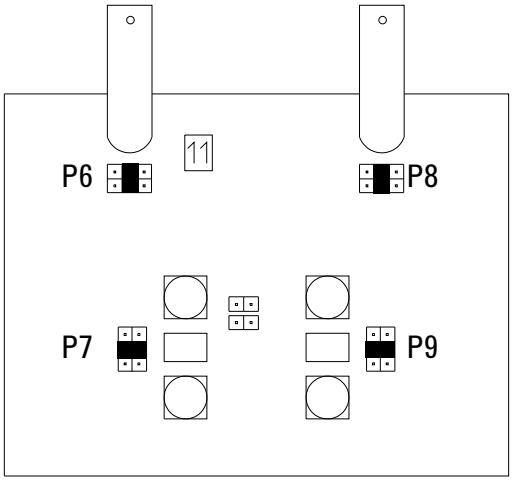
Jumper Positions for Test Fixture Section 11

Filter Bandwidth **Jumper Locations**

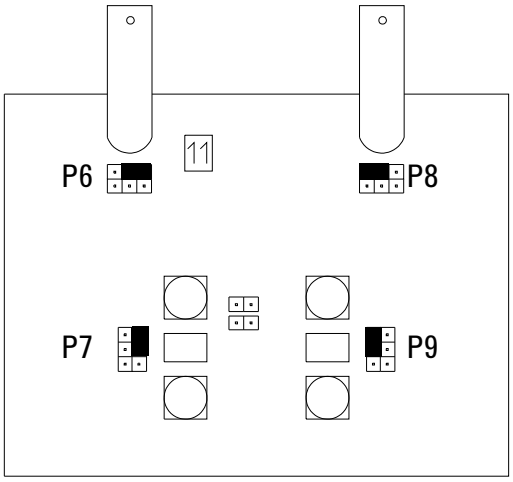
25 MHz



35 MHz



102 MHz



Calibration Setup for Non-33250A Disturbing Signal Source

Before running disturbing signal tests, the disturbing signals need to be calibrated. Connect the equipment as shown in Figure 10, “Calibration Setup the for Non-33250A Disturbing Signal Source,” on page 41 and calibrate the source for Test Mode 1 and Test Mode 4 tests.

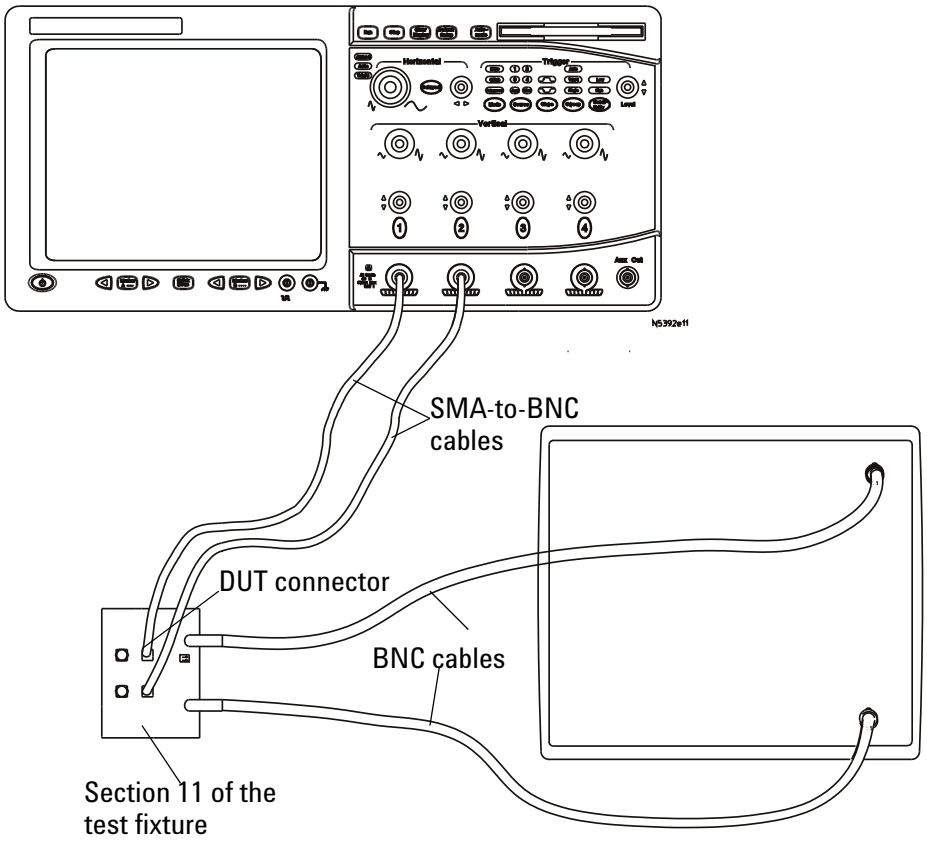


Figure 10 Calibration Setup the for Non-33250A Disturbing Signal Source

Performing the Calibration

1. Select the appropriate filter configuration. Refer to Table 15, “Disturbing Signal Source Settings,” on page 42.
2. Set the source to output a differential signal with an amplitude of V_d and a frequency of F_d. Refer to Table 15 on page 42.
3. Use autoscale feature of the oscilloscope to display the signal.
4. Use the oscilloscope to measure the amplitude and frequency, adjust the disturbing signal source, if needed, to generate an output signal with an amplitude of V_d and a frequency of F_d. Refer to Table 15 on page 42.

5 Phase difference between the differential signal must be exactly 180 degrees. Adjust the phase if required.

6 Save the source configuration for later use.

Table 15 Disturbing Signal Source Settings

Test Mode	Filter configuration	F_d	V_d
Test Mode 1	35Mhz (See page 40)	31.25Mhz	1.4V
Test Mode 4	25Mhz (see page 40)	20.88Mhz	2.7V

Note: V_d is denoted as the amplitude at each channel

Disturbing Signal Probing Setup for Test Mode 1 and Test Mode 4 Using Non-33250A Signal Generators

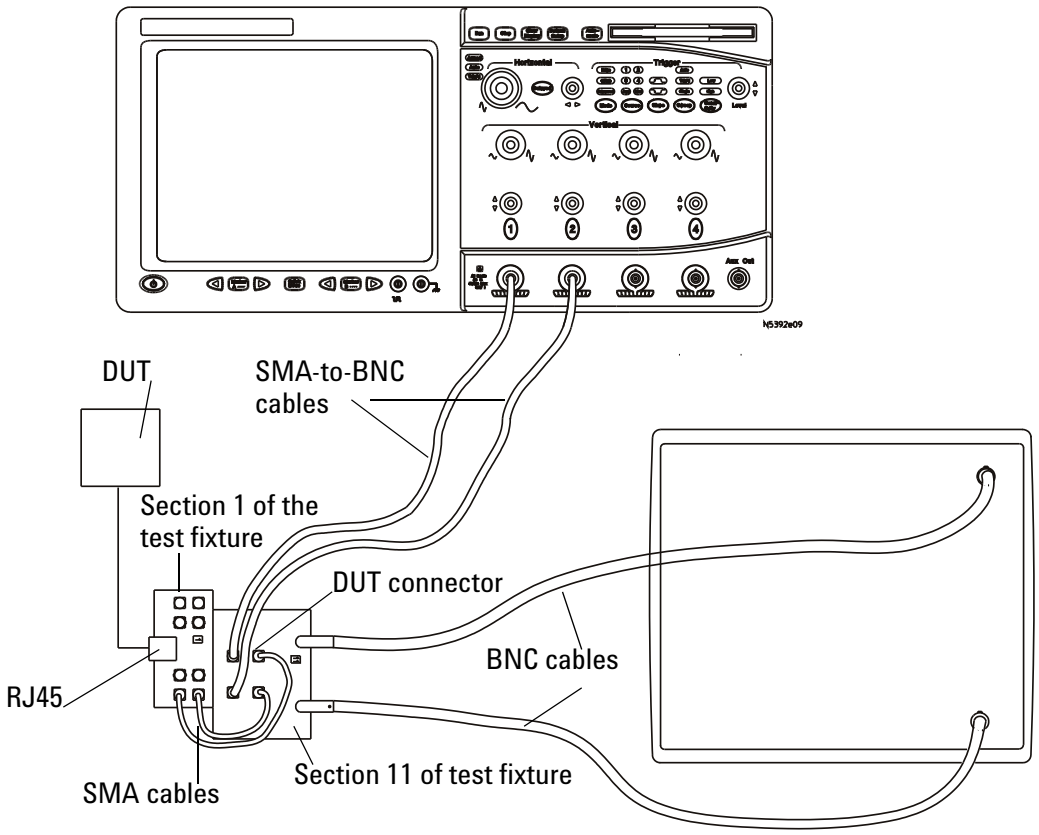


Figure 11 Probing and Cable Connections for Test Mode 1 and Test Mode 4 Using the Non-33250A Signal Generators

Recall the configuration that you have saved during the previous calibration steps, for each test mode. Run the test.

Test Mode 1

Peak Output Voltage Tests

These tests measure the output voltage of points A, B, C, and D of the Test Mode 1 signal at the MDI. This test uses section 2 of the Ethernet test fixture, and applies a 2 MHz high-pass filter in software after acquiring the data. These measurement are made for all 4 pairs (A, B, C, and D)

The allowable ranges for these measurements are as follows:

Table 16 Allowable Ranges for Peak Output Voltage Measurements

Point on Test Mode 1 Signal	Allowable Range	Description
Point A	0.67 V to 0.82 V	Absolute value of Peak A is 0.75 V +/- 0.83 dB
Point B	|Peak B| between 0.67 V and 0.82 V	Absolute value of Peak B is 0.75 V +/- 0.83 dB
Difference A,B	100*[abs(|Peak A|-|Peak B|)/½*(|Peak A|+ |Peak B|)]	Absolute values of amplitude of Peaks A and B differ by less than 1%[1]
Point C	<2% of ½* (|Peak A|+|Peak B|)	Absolute value of Peak C is within 2% of ½ the average amplitude of Peaks A and B[1]
Point D	<2% of ½* (|Peak A|+|Peak B|)	Absolute value of Peak D is within 2% of ½ the average amplitude of Peaks A and B[1]

[1] NOTE: The specified tolerance for this measurement is extremely tight. If this test fails, consult the vertical gain accuracy of your oscilloscope before you draw any conclusions about conformance.

Reference

[1] IEEE 802.3-2008, Subclause 40.6.1.2.1.

Probing Setup

Refer to "Without Disturbing Signal Probing for Test Mode 1 and Test Mode 4" on page 34. This probing configuration is used for all 1000 Base-T Test Mode 1 Signal Tests.

Device Configuration

1 Configure the DUT to output the Test Mode 1 signal.

Using your PHY vendor's provided method, set the DUT's GMII register bits 9.15, 9.14, 9.13 to the values 0, 0, 1 respectively.

2 Ensure that the DUT is transmitting the proper signal as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel
- Capture the waveform around Point A, B, C, or D depending on the Test
- Apply a 2 MHz high-pass filter to this waveform
- Measure the Peak voltage of the waveform at this point.

NOTE

If you have selected "ALL" as the 1000 Base-T, Test Pair (in the "Configure" tab), all 4 pairs will be tested in sequence. You will be prompted to move the probe to the test point for each test pair in turn, and this measurement will be repeated at each of these test points. If you want to debug a particular pair, select the individual pair you wish to test. Note that for full compliance testing, the specification requires testing all 4 pairs. At the result screen, 4 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Test Pair BI_DA result, Trial 2 contains Test Pair BI_DB result and so on.

Algorithm Discussion

Reference [1] defines the peak differential output voltage and level accuracy specifications for a 1000 Base-T device at the physical medium attachment (PMA) sublayer to Media Dependent Interface (MDI). The Peak Voltage tests verify that the Peak Voltages of points A, B, C, and D of the Test Mode 1 signal at the MDI are within the specified range.

The oscilloscope triggers on the appropriate point (A,B,C,D) of the Test Mode 1 signal, as defined in Figure 12. The tests verify that the absolute value of the peak voltage at A and B are in the range of 0.67 V to 0.82 V (0.75 V +/- 0.83 dB). Additionally, the ideal value for the absolute value of the peak voltage at points C and D is one half the average of the peak voltage at points A and B. We measure the absolute value of the peak voltage at points C and D and ensure that they deviate no more than 2% from this ideal voltage.

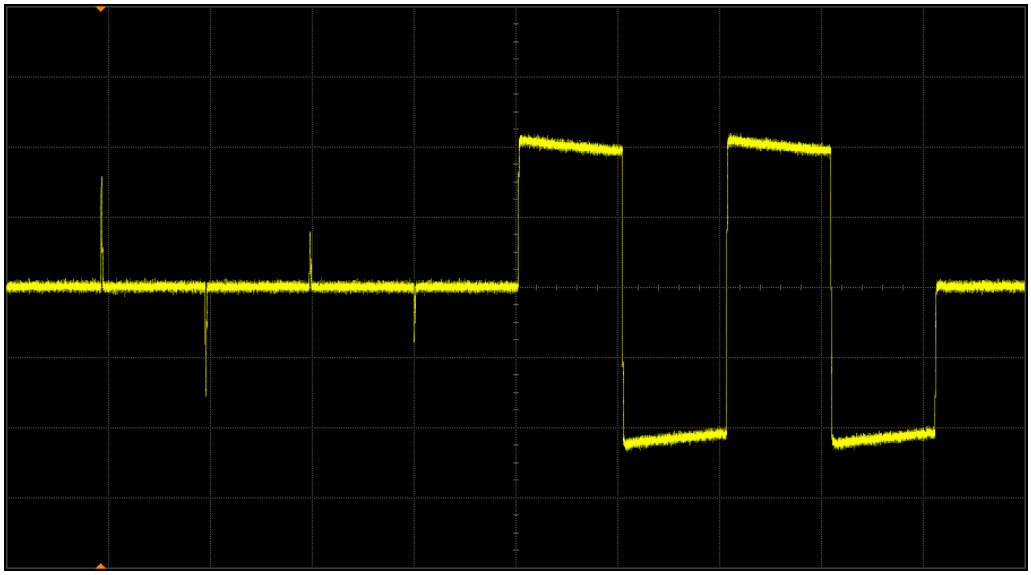


Figure 12 Example of Transmitter Test Mode 1 Waveform (1 Cycle)

Trigger Averaging Notes Reference [1] allows the use of trigger averaging to reduce measurement noise and increase measurement resolution; however, the specification does not provide any constraints on how much averaging may be used.

NOTE In general, averaging may also reduce the effects of real signal variations.

A user-configurable amount of averaging is used. One hundred twenty-eight (128) averages are used by default to reduce the effect of noise on the measurement. You may wish to decrease this number to increase the effects of random signal variations. You may also wish to increase this number to further reduce the effects of noise and increase measurement resolution.

Templates Tests

These tests ensure that the normalized waveform of the Test Mode 1 signal at points A, B, C, D, F, and H as measured at the MDI after being filtered by a 2 MHz high-pass filter, lies within the time domain template defined in Figure 40-26 of Reference [1]. This test uses section 2 of the Ethernet test fixture, and applies a 2 MHz high-pass filter in software after acquiring the data. These measurement are made for all 4 pairs (A, B, C, and D).

Reference

[1] IEEE 802.3-2008, Subclause 40.6.1.2.3.

Probing Setup

Refer to “Without Disturbing Signal Probing for Test Mode 1 and Test Mode 4" on page 34. This probing configuration is used for all 1000 Base-T Test Mode 1 Signal Tests.

Performing the Test

1. Ensure this test is checked to run in the "Select Tests" tab.
2. Press the "Run Tests" button in the task flow to start testing.
3. If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.
4. The test will:
   - Verify that the correct test signal is present on the configured "DUT Data" channel.
   - Capture the waveform around Point A, B, C, D, F, or H depending on the Test.
   - Apply a 2 MHz high-pass filter to this waveform.
   - Normalize the waveform as indicated in Table 17. NOTE: No other vertical adjustments are allowed as per the specification.
   - Shift the waveform in time for the best fit to the specified mask.
   - Capture a number of waveforms (user configurable in the "Configure" tab), testing each waveform against the specified mask, recording failures when they occur.

NOTE

If you have selected "ALL" as the 1000 Base-T, Test Pair (under the "Configure" tab), all 4 pairs will be tested in sequence. You will be prompted to move the probe to the test point for each test pair in turn, and this measurement will be repeated at each of these test points. If you want to debug a particular pair, select the individual pair you wish to test. For full compliance testing, the specification requires testing all 4 pairs. At the result screen, 4 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Test Pair BI_DA result, Trial 2 contains Test Pair BI_DB result and so on.

Algorithm Discussion

Reference [1] describes the differential output template specifications for a 1000 Base-T device at the physical medium attachment (PMA) sublayer to Media Dependent Interface (MDI). These tests ensure that the normalized waveform of the Test Mode 1 signal at points A, B, C, D, F, or H as measured at the MDI after being filtered by a 2 MHz high-pass Filter, lies within the time domain template defined in Figure 40-26 of Reference [1].

The oscilloscope triggers on the appropriate point (A, B, C, D, F, H) of the Test Mode 1 signal, as defined in Figure 12. The software applies a 2 MHz high-pass filter to this waveform. The waveform is then normalized as follows:

Table 17 How Waveforms are Normalized

Point of Test Mode 1 Signal	Normalized by dividing by
Point A	The peak voltage at point A
Point B	The negative of the peak voltage at point A
Point C	½ times the peak voltage at point A
Point D	The negative of ½ times the peak voltage at point A
Point F	The peak voltage at point F
Point H	The negative of the peak voltage at point F

The waveform is shifted in time for the best fit to the specified mask. A number of waveforms are captured, testing each waveform against the specified mask, and recording failures when they occur. There should be no failures for a compliant DUT.

These tests are to be performed on all 4 pairs.

Note that a user configurable amount of trigger averaging is used to reduce measurement noise and increase measurement resolution. See "Trigger Averaging Notes" on page 46 for a discussion of the effects of trigger averaging.

Droop Tests

These tests ensure that the output droop of the differential signal at the MDI output is within conformance limits. Voltage is measured at points F and G, and at points H and J of the Test Mode 1 signal, as indicated in Figure 40-26. The amplitude of the peak voltage at points G and J shall be greater than 73.1% of the amplitude of the peak voltage at points F and H respectively. This test does not use a high-pass filter. This measurement is made for all 4 pairs (A, B, C, and D).

Reference

[1] IEEE 802.3-2008, Subclause 40.6.1.2.2

Performing the Test

1. Ensure this test is checked to run in the "Select Tests" tab.
2. Press the "Run Tests" button in the task flow to start testing.
3. If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.
4. The test will:
   - Verify that the correct test signal is present on the configured "DUT Data" channel.
   - Capture the waveform around points F and G, or points H and J depending on the Test.
   - Measure the minimum/maximum peak voltage at point F/ H respectively. Define this as VPointF or VPointH.
   - Record the time of this peak voltage as TPeakF or TpeakH.
   - Point G is defined as the point exactly 500 ns after point F. Point J is defined as the point exactly 500 ns after Point H. Measure the voltage at point G or H. Define this voltage as VpointG or VpointH respectively.
   - Measure the percentage of point J to point H, or the percentage of point G to point F as:
     - % of G = (VpointG/VpointF)*100%
     - % of J = (VpointJ/VpointH)*100%

NOTE

If you have selected "ALL" as the 1000 Base-T, Test Pair (under the "Configure" tab), all 4 pairs will be tested in sequence. You will be prompted to move the probe to the test point for each test pair in turn, and this measurement will be repeated at each of these test points. If you want to debug a particular pair, select the individual pair you wish to test. For full compliance testing, the specification requires testing all 4 pairs. At the result screen, 4 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Test Pair BI_DA result, Trial 2 contains Test Pair BI_DB result and so on.

Algorithm Discussion

Reference [1] describes the maximum output droop specifications for a 1000 Base-T device at the physical medium attachment (PMA) sublayer to Media Dependent Interface (MDI). These tests ensure that the output droop of the differential signal at the MDI output is within conformance limits.

Voltage is measured at points F and G, and at points H and J of the Test Mode 1 signal, as indicated in Figure 40-26. The amplitude of the peak voltage at points G and J shall be greater than 73.1% of the amplitude of the peak voltage at points F and H respectively. This test does not use a high-pass filter. This measurement is made for all 4 pairs (A, B, C, and D). The algorithm is described in "Performing the Test" on page 50.

NOTE A user configurable amount of trigger averaging is used to reduce measurement noise and increase measurement resolution. See "Trigger Averaging Notes" on page 46 for a discussion of the effects of trigger averaging.

Test Mode 4

This section describes the 1000 Base-T transmitter distortion tests as per IEEE 802.3-2008, Subclause 40.6.1.2.4. The test procedures described in this section cover distortion measurements required by the specification.

When in test mode 4 and observing the differential signal output at the MDI using transmitter test fixture 3, for each pair, with no intervening cable, the peak distortion as defined below shall be less than 10 mV. The peak distortion is determined by sampling the differential signal output with the symbol rate TX_TCLK at an arbitrary phase and processing a block of any 2047 consecutive samples with the MATLAB (see 1.3) code listed below or equivalent. Note that this code assumes that the differential signal has already been filtered by the test filter.

Reference

[1] IEEE 802.3-2008, Subclause 40.6.1.2.4

Device Configuration

1 Configure the DUT to output the Test Mode 4 signal (MASTER timing mode).

   Using your PHY vendor's provided method, set the DUT's GMII register bits 9.15, 9.14, 9.13 to the values 1, 0, 0 respectively.

2 Ensure that the DUT is transmitting the proper signal as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel.
- Capture the signal for n length of time, where n depends on the number of configured averages.
- Analyze the signal and calculate the distortion.

NOTE If you have selected "ALL" as the 1000 Base-T, Test Pair (under the "Configure" tab), all 4 pairs will be tested in sequence. You will be prompted to move the probe to the test point for each test pair in turn, and this measurement will be repeated at each of these test points. If you want to debug a particular pair, select the individual pair you wish to test. For full compliance testing, the specification requires testing all 4 pairs. At the result screen, 4 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Test Pair BI_DA result, Trial 2 contains Test Pair BI_DB result and so on.

Algorithm Discussion

Reference [1] describes how transmitter distortion can be measured by analyzing TM4 signal from a DUT.

The test will analyze the signal using the following steps.

1 Remove the disturbing signal (if it exists).

2 Compensate for fixture losses.

3 Apply 2 MHz test high-pass filter.

4 Extract the clock.

5 Calculate the transmitter distortion.

NOTE A user configurable amount of averaging is used to reduce measurement noise and increase measurement resolution. The default average factor is 150. The average factor also represents the length of data needed to be analyzed, using the following calculation.

$$\text{Length of sampling time} = \frac{2047 \times \#\text{Averages}}{125 \times 10^6}$$

MDI Common Mode Output Voltage

This test ensures that peak-to-peak common mode output voltage at the MDI is within conformance limits. Common Mode voltage is measured over a period of time and the peak-to-peak common mode output voltage is measured as the worst case minimum to worst case maximum common mode output voltage. This test does not use a high-pass filter. This measurement is made for all 4 pairs (A, B, C, and D).

Reference

[1] IEEE 802.3-2008, Subclause 40.8.3.3.

Probing Setup

NOTE Before starting a test, you can view these connection instructions in the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

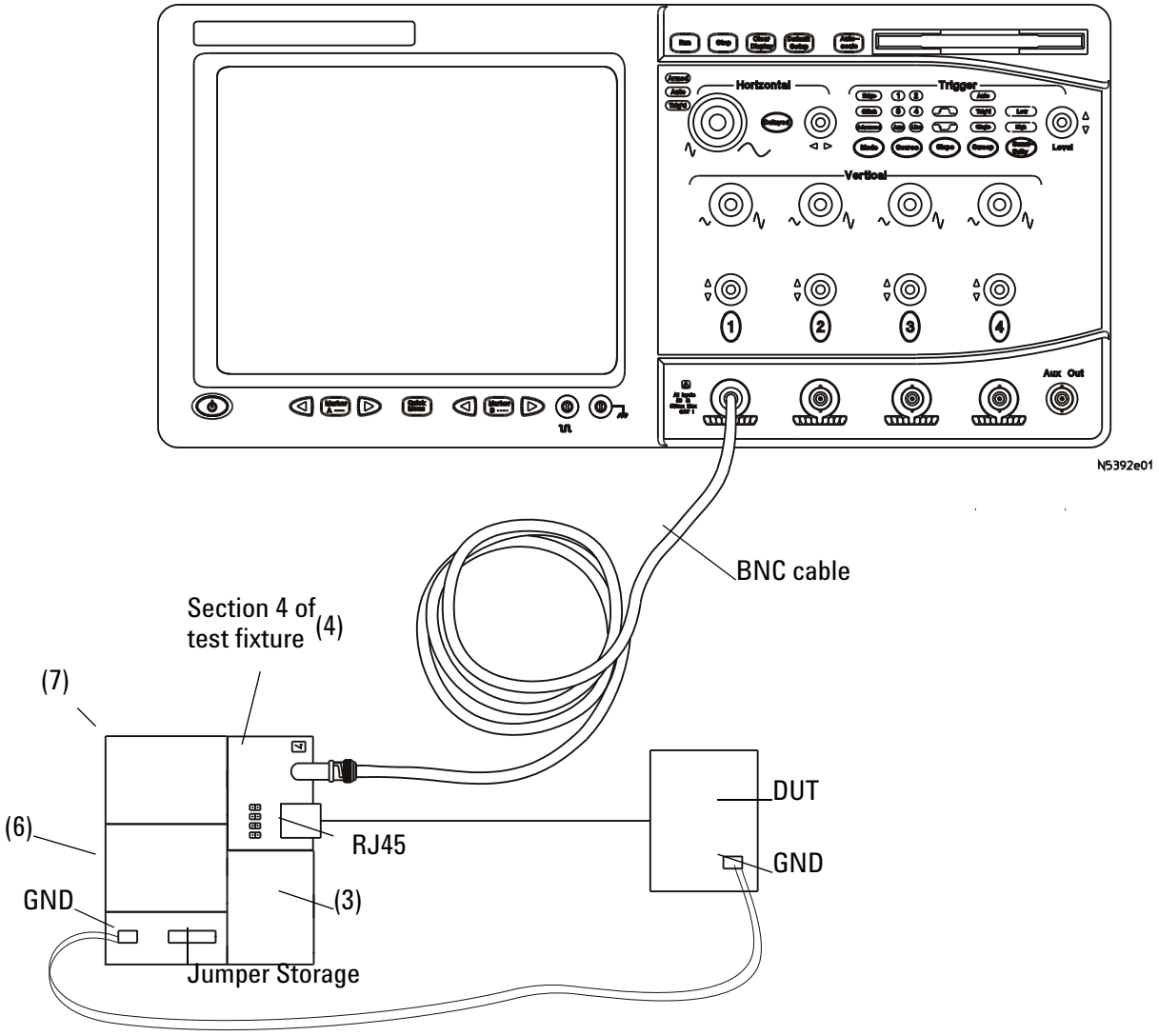


Figure 13 Probing for 1000 Base-T MDI Common Mode Output Voltage

1 Connect the DUT to the RJ45 connector on fixture 4 using a short straight-through UTP cable.

2 Using a single jumper, short the appropriate pins for the pair you are testing on fixture 4 (Pair A, B, C or D).

3 Using a short BNC cable, connect the BNC connector on fixture 4 to the oscilloscope channel selected in the "Configure" tab for “Common Mode BNC”.

4 Connect the ground point of the DUT to the ground point on the fixture with a cable.

Device Configuration

1 Configure the DUT to output the Test Mode 4 signal. An example of this waveform is shown in Figure 14.

   Using your PHY vendor's provided method, set the DUT's GMII register bits 9.15, 9.14, 9.13 to the values 1, 0, 0 respectively.

2 Ensure that the DUT is transmitting the proper signal as indicated in the connection instructions provided in the user interface.

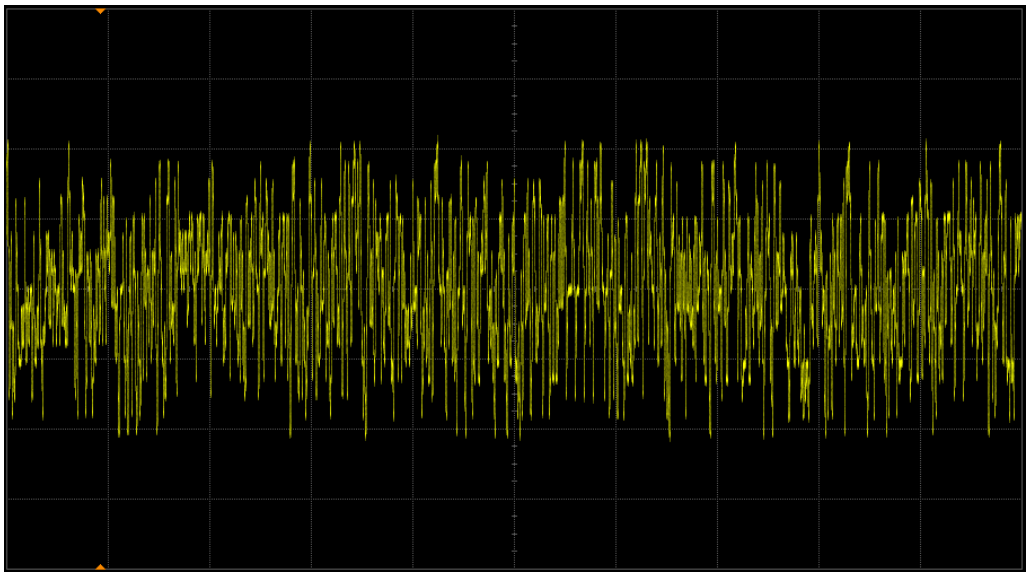


Figure 14 Example of Transmitter Test Mode 4 Waveform (1 Cycle)

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "Common Mode" channel
- Capture multiple acquisitions totaling 100 ms of the common mode output voltage signal Ecm_out test point as shown in figure 40-32. Display this signal as a color-graded persistence waveform.

- Record the worst case minimum and maximum voltage encountered over all acquired data.
- Compute the worst case peak-to-peak common mode output voltage as the worst case maximum voltage minus the worst case minimum voltage.

NOTE

If you have selected "ALL" as the 1000 Base-T, Test Pair (under the "Configure" tab), all 4 pairs will be tested in sequence. You will be prompted to move the probe to the test point for each test pair in turn, and this measurement will be repeated at each of these test points. If you want to debug a particular pair, select the individual pair you wish to test. For full compliance testing, the specification requires testing all 4 pairs. At the result screen, 4 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Test Pair BI_DA result, Trial 2 contains Test Pair BI_DB result and so on.

Algorithm Discussion

Reference [1] describes the maximum transmitter common mode voltage specifications for a 1000 Base-T device at the Media Dependent Interface (MDI). The total Common Mode voltage Ecm_out as indicated in Figure 15 is measured over a 100 ms duration and the peak-to-peak common mode output voltage is measured as the worst case minimum to worst case maximum common mode output voltage. This test does not use a high-pass filter. This measurement is made for all 4 pairs (A, B, C, and D).

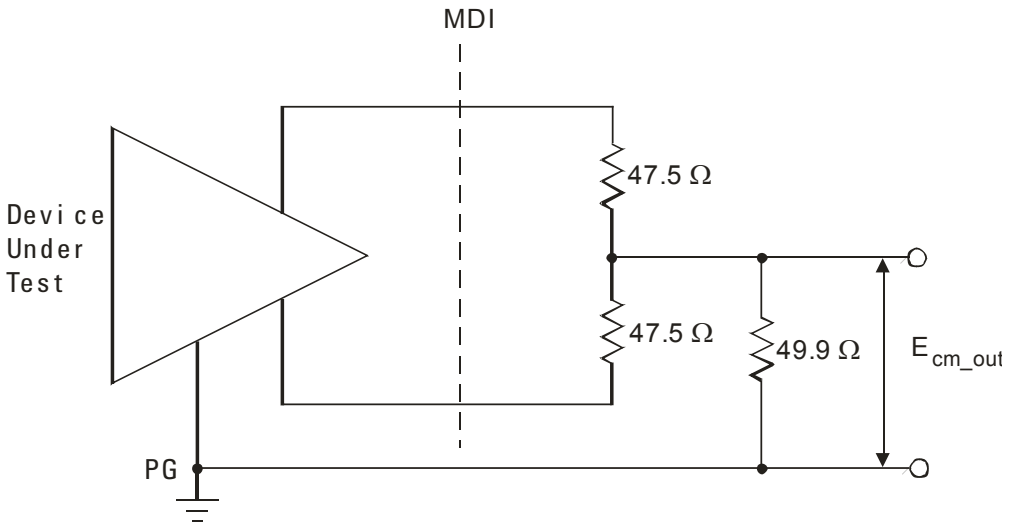


Figure 15 Common Mode Output Voltage Test Circuit

Jitter Tests with TX_TCLK, DUT in MASTER Mode

This section describes the 1000 Base-T jitter tests as per IEEE 802.3-2008, Subclause 40.6.1.2.5. The test procedures described in this section cover jitter measurements required by the specification.

The following jitter tests are performed for 1000 Base-T devices with the DUT in MASTER mode:

MASTER Mode JTxOut Measures the jitter on the MDI data relative to the DUT transmit clock (TX_TCLK) for pair A,B,C and D, while in MASTER timing mode. Though these measurements indirectly impact conformance, there are no specific conformance limits. The results are reported for informative purposes.

Jitter MASTER Unfiltered Measures the jitter on the DUT transmit clock (TX_TCLK) signal relative to an *unjittered reference* while in the MASTER timing mode.

Jitter MASTER Filtered Measures the jitter on the DUT transmit clock (TX_TCLK) signal relative to an *unjittered reference* while in the MASTER timing mode, after being filtered by a 5 kHz high-pass filter. This test also uses the worst MASTER JTxOut measurement results.

NOTE For full conformance testing, unfiltered jitter measurements require 12.5 million edges. This can take up to about 8 minutes per unfiltered jitter measurement. For a quicker estimate of the health of a DUT, you may wish to reduce the number of unfiltered jitter edges in the "Configure" tab.

MASTER Mode JTxOut

The MASTER mode JTxOut measurements are used to measure the jitter on the MDI signal relative to the transmit clock (TX_TCLK) of the DUT. Though these measurements indirectly impact conformance, there are no specific conformance limits specified. JTxOut is measured on pairs A, B, C, and D. This produces 4 distinct MASTER JTxOut results. The results are reported for informative purposes.

Reference

[1] IEEE 802.3-2008, Subclause 40.6.1.2.5.

Probing Setup

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

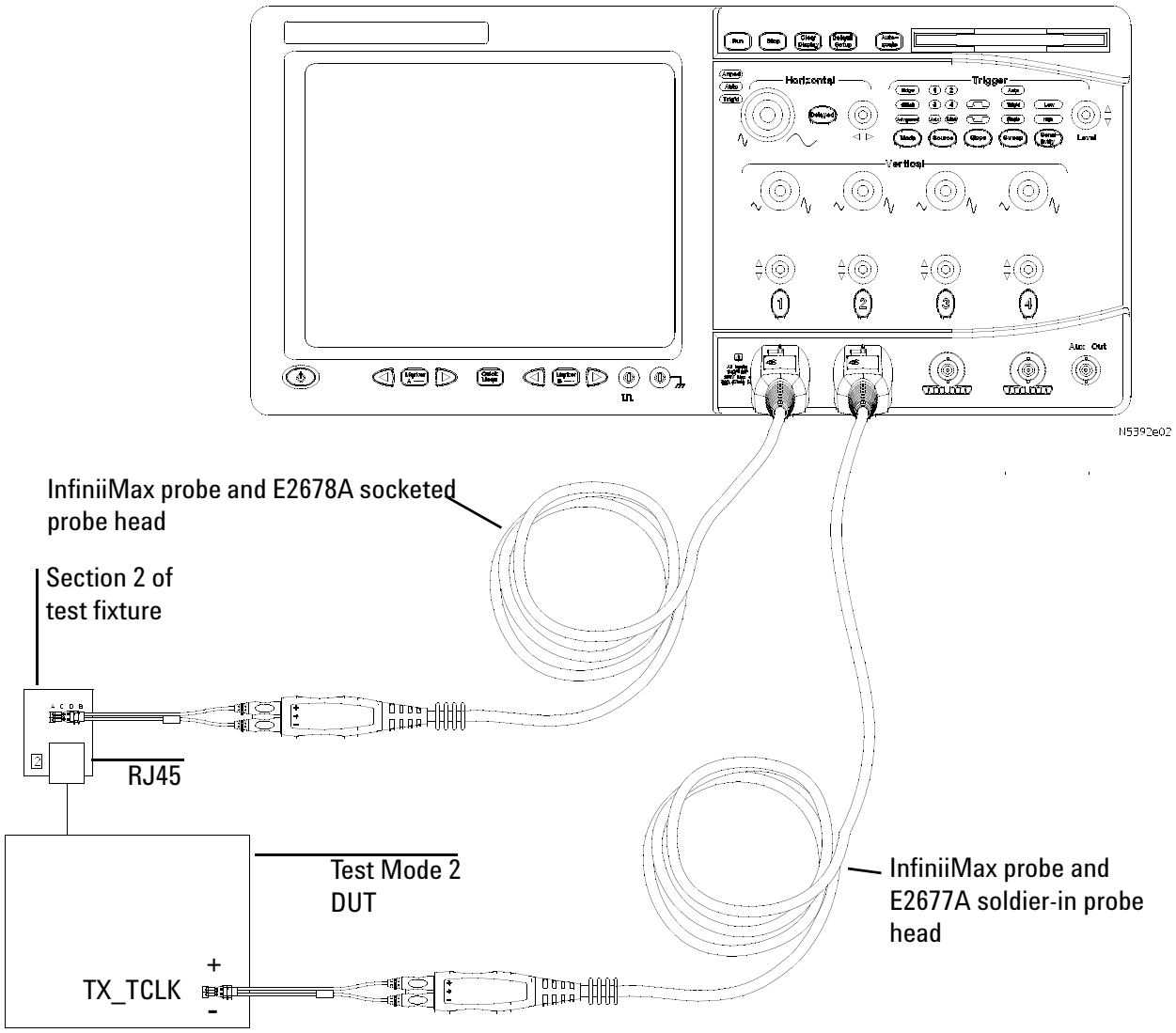


Figure 16 Probing for 1000 Base-T MASTER JTxOut

1 Connect the DUT to the RJ45 connector on fixture 2 using a short straight-through UTP cable.

2 Connect an InfiniiMax differential probe with the E2678A differential socketed probe head to the test point for the pair you are testing (A, B,

C, or D) on fixture 2, and to the configured “DUT Data” Channel on the oscilloscope.

3 Connect a second InfiniiMax probe with E2677A differential solder-in probe head to the transmit clock (TX_TCLK) on the DUT and to configured “DUT TX_TCLK Channel” on the oscilloscope.

Device Configuration

1 Configure the DUT to output the Test Mode 2 signal (MASTER timing mode).

Using your PHY vendor's provided method, set the DUT's GMII register bits 9.15, 9.14, 9.13 to the values 0, 1, 0 respectively.

2 Ensure that the DUT is transmitting the proper signal as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signals are present on the configured "DUT Data" channel and "DUT TX_TCLK" channel.
- Configure the oscilloscope and simultaneously capture 100 ms to 1 second of the MDI data of the current pair and DUT transmit clock (TX_TCLK) signal.
- Compute JTxOut as described in the Algorithm Discussion below.

NOTE

If you have selected "ALL" as the 1000 Base-T, Test Pair (under the "Configure" tab), all 4 pairs will be tested in sequence. You will be prompted to move the probe to the test point for each test pair in turn, and this measurement will be repeated at each of these test points. If you want to debug a particular pair, select the individual pair you wish to test. For full compliance testing, the specification requires testing all 4 pairs. At the result screen, 4 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Test Pair BI_DA result, Trial 2 contains Test Pair BI_DB result and so on.

Algorithm Discussion

Reference [1] describes all the transmitter timing jitter specifications for a 1000 Base-T device at the physical medium attachment (PMA) sublayer to Media Dependent Interface (MDI). JTxOut is defined as the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of the DUT transmit clock (TX_TCLK).

JTxOut is a basically a measurement of the jitter on the data signal at the MDI relative to the DUT's transmit clock (TX_TCLK). The specification distinguishes MASTER (Test Mode 2) and SLAVE (Test Mode 3) timing mode JTxOut measurements. Because JTxOut must measure jitter on the data, we must measure JTxOut for all 4 pairs. This results in 4 MASTER mode JTxOut measurements.

Reference [1] does not define any conformance requirements for JTxOut. However, JTxOut is used to determine compliance when combined with filtered jitter measurements, and therefore ultimately affects conformance. The JTxOut measurement results are reported for informative purposes.

As indicated in Figure 16, both the DUT TX_TCLK signal and the MDI data signal are connected to the oscilloscope. Because JTxOut is an unfiltered jitter measurement, we must observe not less than 100 ms worth of data and not more than 1 second of data, as stated in Reference [1]. This corresponds to a minimum of 12.5 million symbol times. The algorithm proceeds as follows:

1. Simultaneously capture a long record with both signals (MDI data and DUT TX_TCLK).
2. Define reference edge times as the 50% threshold crossings of the selected edge (rising or falling) of the TX_TCLK signal.
3. Define a jitter quantity, measured from the reference edge time of TX_TCLK to the 0 V crossing of the selected edge of the MDI data signal. The jitter result for each edge on the MDI data signal is added to a jitter histogram for visualization purposes.
4. Steps 1 to 3 are repeated to acquire new data and accumulate the jitter histogram with each new acquisition until at least 100 ms of data has been analyzed.
5. The peak-to-peak value over the entire multi-acquisition jitter population is recorded as JTxOut.
6. If ALL pairs are being tested steps 1-5 are repeated for each pair.
7. The worst-case JTxOut value (over all pairs) is recorded as the worst MASTER JTxOut value.

NOTE This worst-case value will be used later in the "Jitter Master Filtered" test to determine conformance.

Jitter MASTER Unfiltered

The unfiltered DUT TX_TCLK Jitter test is used to ensure that the jitter on the DUT's transmit clock (TX_TCLK) relative to an *unjittered reference* is less than 1.4 ns.

Reference

[1] IEEE 802.3-2008, Subclause 40.6.1.2.5

Probing Setup

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

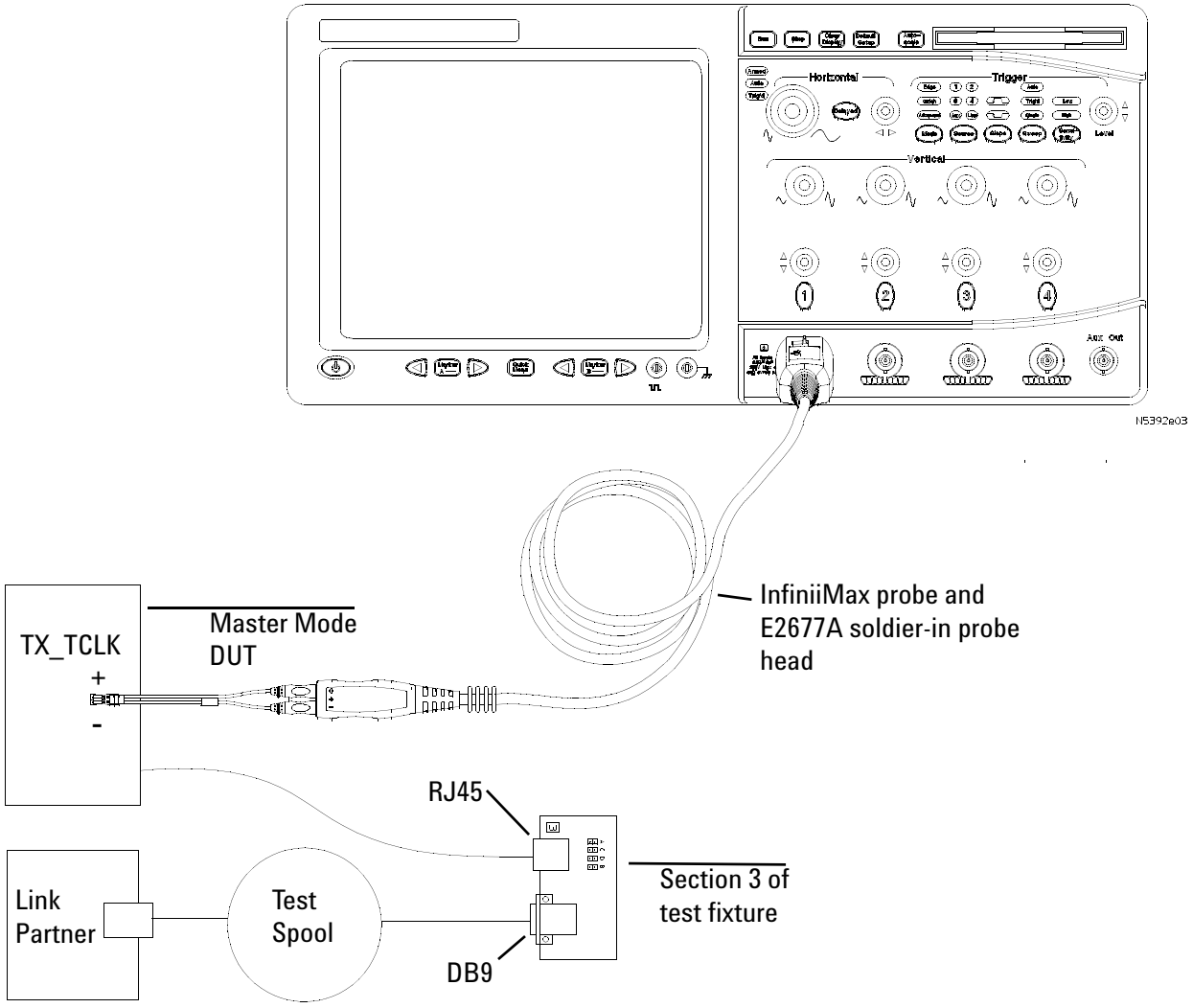


Figure 17 Probing for 1000 Base-T MASTER TX_TCLK Jitter (Filtered and Unfiltered)

1 Connect the DUT to the RJ45 connector on fixture 3 using a short straight-through UTP cable.

2 Connect the Link Partner to the DB9 connector on fixture 3 with the Test Channel.

3 Connect an InfiniiMax differential probe with E2677A differential solder-in probe head to the transmit clock (TX_TCLK) on the DUT and to the configured “DUT TX_TCLK” channel on the oscilloscope.

Device Configuration

1 Configure the DUT to operate normally in the MASTER timing mode.
   a Reset both the DUT and the Link-Partner devices if necessary
   b Using your PHY vendor's provided method, set the following GMII register bits:
      • Set bit 9.12 to enable MASTER-SLAVE Manual Configuration.
      • Set bit 9.11 to force the DUT to become the MASTER.
2 Ensure that the Link Partner is properly receiving data from the DUT by verifying that the Link Partner has set its GMII register bit 10.13 is set to 1.
3 Ensure that the DUT is transmitting the proper signal as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.
2 Press the "Run Tests" button in the task flow to start testing.
3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.
4 The test will:
   • Verify that the correct test signal is present on the configured "DUT TX_TCLK" channel.
   • Capture 100 ms to 1 second of the DUT TX_TCLK signal.
   • Compute the peak-to-peak unfiltered MASTER TX_TCLK jitter as described in the Algorithm Discussion below, and confirm that this value is less than 1.4 ns.

Algorithm Discussion

Reference [1] describes all the transmitter timing jitter specifications for a 1000 Base-T device at the physical medium attachment (PMA) sublayer to Media Dependent Interface (MDI). This section states that when in the normal mode of operation as the MASTER, the peak-to-peak value of the MASTER TX_TCLK jitter relative to an *unjittered reference* shall be less than 1.4 ns.

This test is a measurement of the jitter on the DUT's transmit clock (TX_TCLK) relative to an *unjittered reference*. The *unjittered reference* is a assumed to be a computed ideal clock waveform with no jitter. The method for computing this *unjittered reference* is described in the algorithm procedure below.

The specification does not define the term *unjittered reference*. We define a derived *unjittered reference* from the actual TX_TCLK signal as follows:

- Measure all timing instants (at the 50% crossing points) of the actual clock signal over a long record.
- Compute the mean frequency of this measured clock signal over the entire record.
- An ideal clock signal is constructed as a jitterless clock signal with the frequency of the computed mean frequency of the actual clock signal. The phase of this clock is chosen to minimize the difference from the timing instants of the ideal clock to the actual timing instants of the measured clock.
- The jitter of each measured timing instant of the actual clock signal is computed as the deviation from the corresponding timing instant of the computed ideal clock.

Reference [1] states that all peak-to-peak unfiltered jitter measurements shall be made over an interval not less than 100 ms and not more than 1 second. This corresponds to a minimum of 12.5 million symbol times.

As indicated in Figure 17, only the DUT TX_TCLK signal is connected to the oscilloscope. The algorithm proceeds as follows:

1. Capture a long record of the DUT TX_TCLK signal.
2. Compute ideal clock instants as discussed above.
3. Define a jitter quantity, for each measured timing instant of DUT TX_TCLK signal, as the deviation of the 50% crossing of the TX_TCLK signal to the its corresponding ideal clock edge.
4. The jitter value for each edge on DUT TX_TCLK signal is added to a jitter histogram for purposes of understanding and visualizing the distribution of jitter.
5. Steps 1 to 4 are repeated to acquire new data and accumulate the jitter histogram with each new acquisition until at least 100 ms of data has been analyzed.
6. The peak-to-peak value over the entire multi-acquisition jitter population is recorded as the unfiltered MASTER TX_TCLK jitter.

Jitter MASTER Filtered

Reference [1] describes all the transmitter timing jitter specifications for a 1000 Base-T device at the physical medium attachment (PMA) sublayer to Media Dependent Interface (MDI). This section states that when the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf1}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus JTxOut shall be less than 0.3 ns.

$$H_{jf1}(f) = \frac{jf}{jf + 5000} = f \text{ in Hz}$$

The "jitter waveform on TX_TCLK" is defined as the jitter of the MASTER TX_TCLK signal relative to an *unjittered reference* as defined in the algorithm section for MASTER Unfiltered DUT TX_TCLK Jitter.

The filtered DUT TX_TCLK Jitter test ensures that the filtered jitter on the DUT's transmit clock (TX_TCLK) relative to an *unjittered reference* plus the worst case MASTER mode JTxOut (over all pairs) is less than 0.3 ns.

Reference

[1] IEEE 802.3-2008, Subclause 40.6.1.2.5.

Probing Setup

Same as for Jitter MASTER Unfiltered, see "Probing Setup" on page 62.

Device Configuration

Same as for Jitter MASTER Unfiltered, see "Device Configuration" on page 64.

Performing the Test

1. Ensure this test is checked to run in the "Select Tests" tab.
2. Press the "Run Tests" button in the task flow to start testing.
3. If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.
4. The test will:
   - Verify that the correct test signal is present on the configured "DUT TX_TCLK" channel
   - Capture at least 100,000 edges of the DUT TX_TCLK signal.

- Compute a user-configurable jitter waveform of the DUT TX_TCLK relative to an *unjittered reference* as described in the algorithm discussion for MASTER Unfiltered DUT TX_TCLK Jitter.

- Filter the jitter waveform with a 5 kHz high-pass filter.
  - Compute the peak-to-peak value of the filter jitter waveform. For purposes of this section, call this the 5 kHz-filtered MASTER clock jitter.
  - Confirm that the 5 kHz-filtered MASTER clock jitter plus the worst case MASTER mode JTxOut is less than 0.3 ns.
  - See Algorithm Discussion below for further detail.

Algorithm Discussion

Reference [1] describes jitter specifications for a 1000 Base-T device. This section discusses algorithms for measuring filtered DUT TX_TCLK MASTER mode jitter. The unfiltered DUT TX_TCLK MASTER mode jitter is a measurement of the jitter on the DUT's transmit clock (TX_TCLK) relative to an *unjittered reference*. This is a single clock jitter measurement made while the DUT is operating in MASTER timing mode. The unfiltered jitter measurement produces a jitter waveform. The filtered DUT TX_TCLK measurement is a peak-to-peak jitter measurement made on this jitter waveform, after it is filtered with a 5 kHz high-pass filter.

Reference [1] states that all peak-to-peak filtered jitter measurements shall be made over an unbiased sample of at least 100,000 clock edges.

As indicated in Figure 17, only the DUT TX_TCLK signal is connected to the oscilloscope. The algorithm proceeds as follows:

1. Capture at least 100,000 edges of the DUT TX_TCLK signal in one long record.
2. Compute the jitter waveform of the DUT TX_TCLK relative to an *unjittered reference*. The unfiltered jitter waveform is defined as J-DUT-TX_TCLK-MASTER and the method for computing it is described in the "Algorithm Discussion" on page 64.
3. Filter this jitter waveform with a 5 kHz high-pass filter to produce a filtered jitter waveform. For discussion purposes, call this J-DUT-TX_TCLK-MASTER-5K.
4. Ensure that the peak-to-peak value of the filter jitter waveform J-DUT-TX_TCLK-MASTER-5K plus the worst case MASTER mode JTxOut is less than 0.3 ns.

Jitter Tests with TX_TCLK, DUT in SLAVE Mode

This section describes the 1000 Base-T jitter tests as per IEEE 802.3-2008, Subclause 40.6.1.2.5. The tests procedures described in this section cover jitter measurements required by the specification.

The following jitter tests are performed for 1000 Base-T devices with the DUT in SLAVE mode:

SLAVE Mode JTxOut Measures the jitter on the MDI data relative to the DUT transmit clock (TX_TCLK) for pair A,B,C and D, while in SLAVE timing mode. Though these measurements indirectly impact conformance, there are no specific conformance limits. The results are reported for informative purposes

Jitter SLAVE Unfiltered Measures the unfiltered jitter on the DUT transmit clock (TX_TCLK) signal relative to a link-partner's MASTER transmit clock (TX_TCLK). This test is performed while the DUT is operating normally as the SLAVE, connected to a link partner operating as the MASTER via the Test Channel.

Jitter SLAVE Filtered Measures the same jitter quantity (DUT SLAVE TX_TCLK relative to MASTER TX_TCLK) after filtering the jitter with a 32 kHz high-pass filter. This test also simultaneously measures the jitter on the MASTER TX_TCLK relative to an *unjittered reference* after filtering this jitter with a 5 kHz high-pass filter. This test also uses the worst SLAVE JTxOut measurement to determine compliance.

SLAVE Mode JTxOut

The SLAVE mode JTxOut measurements are used to measure the jitter on the MDI signal relative to the transmit clock (TX_TCLK) of the DUT. Though these measurements indirectly impact conformance, there are no specific conformance limits specified. JTxOut is measured on pairs A, B, C, and D. This produces 4 distinct SLAVE JTxOut results. The results are reported for informative purposes.

Reference

[1] IEEE 802.3-2008, Subclause 40.6.1.2.5.

Probing Setup

NOTE

Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

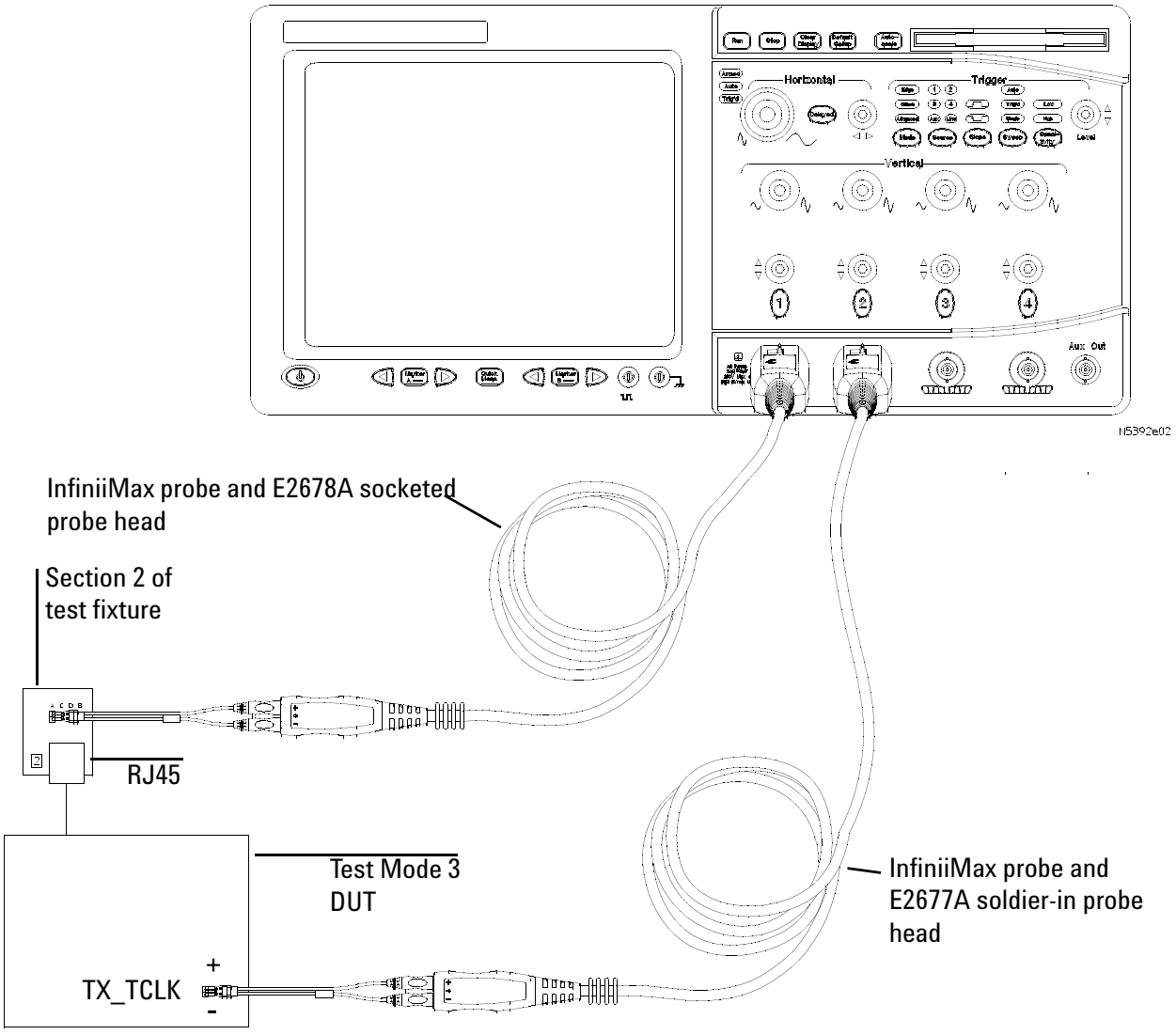


Figure 18 Probing for 1000 Base-T SLAVE JTxOut

Device Configuration

1 Configure the DUT to output the Test Mode 3 signal (SLAVE timing mode).

   Using your PHY vendor's provided method, set the DUT's GMII register bits 9.15, 9.14, 9.13 to the values 0, 1, 1 respectively.

2 Ensure that the DUT is transmitting the proper signal as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signals are present on the configured "DUT Data" channel and "DUT TX_TCLK" channel.
- Configure the oscilloscope and simultaneously capture 100 ms to 1 second of the MDI data of the current pair and DUT TX_TCLK signal.
- Compute JTxOut as described in the Algorithm Discussion below.

NOTE If you have selected "ALL" in the 1000 Base-T, Test Pair configuration option, all 4 pairs will be tested in sequence. You will be prompted to move the probe to each test point in turn, and this measurement will be repeated for each pair. If you are debugging a particular pair, select the individual pair you wish to test. At the result screen, 4 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Test Pair BI_DA result, Trial 2 contains Test Pair BI_DB result and so on.

Algorithm Discussion

The algorithm for this measurement is identical to the algorithm for MASTER JTxOut measurements, with the exception that the DUT is set to operate in SLAVE timing mode (Test Mode 3).

Jitter SLAVE Unfiltered

The unfiltered DUT TX_TCLK Jitter test is used to ensure that, while operating in the SLAVE timing mode, the jitter on the DUT's transmit clock (TX_TCLK) relative to the transmit clock (TX_TCLK) of a Link-Partner operating in the MASTER timing mode is less than 1.4 ns.

Reference

[1] IEEE 802.3-2008, Subclause 40.6.1.2.5.

Probing Setup

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

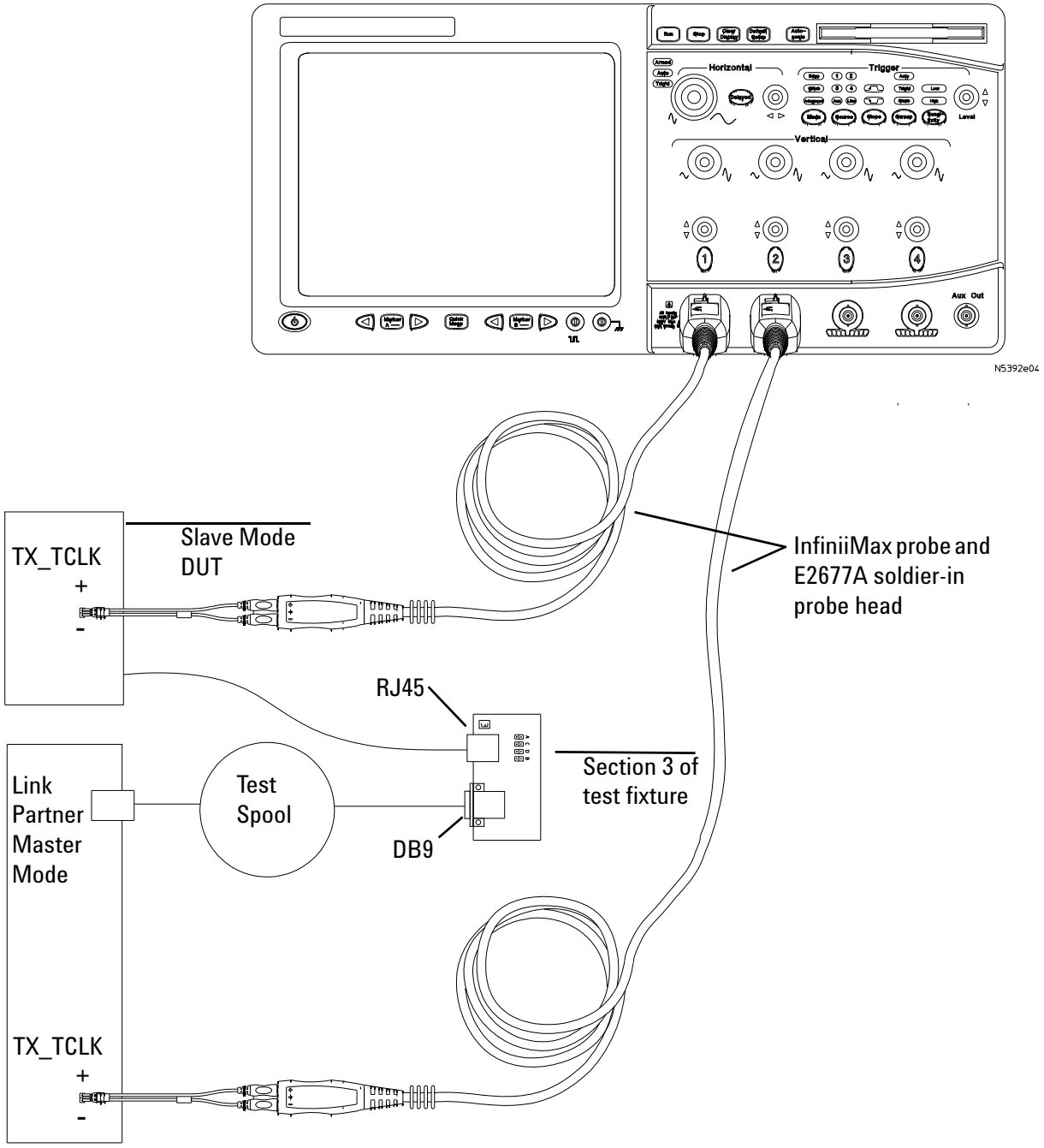


Figure 19 Probing for 1000 Base-T SLAVE TX_TCLK Jitter (Filtered and Unfiltered)

1 Connect the DUT to the RJ45 connector on fixture 3 using a short straight-through UTP cable.

2 Connect the Link Partner to the DB9 connector on fixture 3 with the Test Channel.

3 Connect an InfiniiMax differential probe with E2677A differential solder-in probe head to the transmit clock (TX_TCLK) on the DUT and to the configured “DUT TX_TCLK” channel on the oscilloscope.

4 Connect a second InfiniiMax probe with E2677A differential solder-in probe head to the transmit clock (TX_TCLK) on the Link Partner and to the configured “LP TX_TCLK” channel on the oscilloscope.

Device Configuration

1 Reset both the DUT and the Link-Partner devices if necessary.

2 Ensure that a valid link exists between the DUT and the Link Partner.

3 Configure the Link Partner to operate normally in the MASTER timing mode.

   Using your PHY vendor's provided method, set the following GMII register bits:

   - Set bit 9.12 to enable MASTER-SLAVE Manual Configuration.
   - Set bit 9.11 (to 1) to force the Link Partner to become the Master.

4 Configure the DUT to operate normally in the SLAVE timing mode.

   - Reset both the DUT and the Link-Partner devices if necessary.
   - Using your PHY vendor's provided method, set the following GMII register bits:
     - Set bit 9.12 to enable MASTER-SLAVE Manual Configuration.
     - Clear bit 9.11 (to 0) to force the DUT to become the SLAVE.

5 Ensure that the DUT is properly receiving data from the Link Partner by verifying that the DUT has set its GMII register bit 10.13 is set to 1.

6 Ensure that both TX_TCLK signals (DUT and Link-Partner) are being captured and that their phase relationship is relatively stable over multiple acquisitions. This indicates that the SLAVE clock is tracking the MASTER.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that a worst-case value for SLAVE mode JTxOut has been computed. If this is not the case, the application will prompt you to change the connection and will make these measurements first.
- Verify that the correct test signals are present on the configured "DUT TX_TCLK" and "LP TX_TCLK" channels.
- Simultaneously capture 100 ms to 1 second of the DUT TX_TCLK and Link Partner TX_TCLK signals.
- Compute the peak-to-peak jitter on the SLAVE (DUT) TX_TCLK relative to the MASTER (Link Partner) TX_TCLK as described in the algorithm discussion. Ensure that this value is less than 1.4 ns.

Algorithm Discussion

Reference [1] describes jitter specifications for a 1000 Base-T device. This section discusses algorithms for measuring unfiltered SLAVE mode TX_TCLK jitter of the DUT. This test is carried out while the DUT is operating in SLAVE timing mode, connected to a link partner operating in MASTER timing mode with the jitter test channel. The test measures the peak-to-peak jitter on the DUT's transmit clock (TX_TCLK) relative to the MASTER transmit clock (TX_TCLK). This is a two clock jitter measurement.

Reference [1] states that all peak-to-peak unfiltered jitter measurements shall be made over an interval not less than 100 ms and not more than 1 second. This corresponds to 12.5 million clock periods.

Though the connectivity of this test is quite complex, the measurement algorithm is relatively simple. We define ideal reference edges as the 50% threshold crossings of the MASTER (link partner) TX_TCLK signal. For each rising edge of the DUT TX_TCLK, we compute the difference between the 50% crossing of the DUT TX_TCLK signal and its reference edge.

As indicated in Figure 19, both the DUT TX_TCLK and the link partner TX_TCLK signals are connected to the oscilloscope. The algorithm proceeds as follows:

1. Simultaneously capture a long record of the DUT TX_TCLK and the link partner TX_TCLK signals.
2. Define reference edges for a jitter measurement as the 50% threshold crossing times of the MASTER (link-partner) TX_TCLK signal.
3. Define a jitter quantity, measured for each rising edge of DUT TX_TCLK signal, as the time difference between the 50% crossing of the TX_TCLK signal to the time of its corresponding reference edge. The jitter result for each rising edge on DUT TX_TCLK signal is added to a jitter histogram.
4. Steps 1 to 3 are repeated to acquire new data and accumulate the jitter histogram with each new acquisition until at least 100 ms of data has been analyzed.

5 The peak-to-peak value over the entire jitter population is recorded as J-DUT-TX-TCLK-SLAVE.

6 Ensure that this value is less than 1.4 ns.

Jitter SLAVE Filtered

With the DUT operating in the SLAVE timing mode and a Link-Partner operating in the MASTER timing mode, the filtered DUT TX_TCLK Jitter test is used to ensure that the jitter on the DUT's transmit clock (TX_TCLK, after being filtered with a 32 kHz high-pass filter) is no more than 0.4 ns greater than the simultaneously measured peak-to-peak jitter on the Link-Partner's transmit clock (TX_TCLK, after being filtered by a 5 kHz high-pass filter).

Reference

[1] IEEE 802.3-2008, Subclause 40.6.1.2.5.

Probing Setup

Same as for Jitter SLAVE Unfiltered, see "Probing Setup" on page 71.

Device Configuration

Same as for Jitter SLAVE Unfiltered, see "Device Configuration" on page 73.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that a worst-case value for SLAVE mode JTxOut has been computed. If this is not the case, the application will prompt you to change the connection and will make these measurements first.
- Verify that the correct test signals are present on the configured "DUT TX_TCLK" and "LP TX_TCLK" channels.
- Simultaneously capture at least 100,000 edges of the DUT TX_TCLK and Link Partner TX_TCLK signals.

- Compute a jitter waveform of the SLAVE (DUT) TX_TCLK signal relative to the MASTER (link partner) TX_TCLK signal as described in the algorithm discussion for SLAVE Unfiltered DUT TX_TCLK Jitter.
- Filter this jitter waveform with a 32 kHz high-pass filter. Call the filtered waveform J-DUT-TX-TCLK-SLAVE-32K
- Compute a jitter waveform of the MASTER (link-partner) TX_TCLK signal relative to an *unjittered reference* as described previously in this document.
- Filter this jitter waveform with a 5 kHz high-pass filter. Call the resulting filtered jitter waveform J-LP-TX-TCLK-MASTER-5K.
- Confirm that the worst case SLAVE mode JTxOut plus peak-to-peak (J-DUT-TX-TCLK-SLAVE-32K) minus peak-to-peak (J-LP-TX-TCLK-MASTER-5K) is less than 0.4 ns.
- See Algorithm Discussion below for further detail.

Algorithm Discussion

Reference [1] describes jitter specifications for a 1000 Base-T device. This section discusses algorithms for measuring filtered SLAVE mode TX_TCLK jitter of the DUT. This test is carried out while the DUT is operating in SLAVE timing mode, connected to a link partner operating in MASTER timing mode with the jitter test channel. The test measures a number of parameters as described below. One measurement is the filtered jitter on the MASTER (link partner) TX_TCLK itself relative to an *unjittered reference*. Another measurement is the filtered peak-to-peak jitter on the DUT's transmit clock (TX_TCLK) relative to the MASTER transmit clock (TX_TCLK).

Reference [1] states that all peak-to-peak filtered jitter measurements shall be made over an unbiased sample of at least 100,000 clock edges.

Section "Jitter SLAVE Unfiltered" on page 70 discusses the computation of an unfiltered jitter waveform of the SLAVE (DUT) TX_TCLK relative to the MASTER (link partner) TX_TCLK signal. We simultaneously capture the DUT TX_TCLK and the link-partner TX_TCLK signals and compute such a jitter waveform. We filter this jitter waveform with a 32 kHz high-pass filter to produce a filtered jitter waveform called J-DUT-TX-TCLK-SLAVE-32K.

We also compute another jitter waveform from the simultaneously captured MASTER (link partner) TX_TCLK signal. This jitter waveform is computed relative to an *unjittered reference* (using the mean frequency of the same clock signal, as described elsewhere in this document). We filter this jitter waveform with a 5 kHz high-pass filter to produce a filtered jitter waveform called J-LP-TX-TCLK-MASTER-5K.

As we have defined the jitter waveform names here, the terms of the conformance specification are that J-DUT-TX_TCLK-SLAVE-32K plus the worst SLAVE mode JTxOut must be less than 0.4 ns plus J-LP-TX-TCLK-MASTER-5K.

This constraint can also be expressed as follows, and we do so in this application: J-DUT-TX-TCLK-SLAVE-32K plus the worst SLAVE mode JTxOut minus J-LP-TX-TCLK-MASTER-5K must be less than 0.4 ns.

As indicated in Figure 19, both the DUT TX_TCLK and the link partner TX_TCLK signals are connected to the oscilloscope. The algorithm proceeds as follows:

1. Simultaneously capture a long record of at least 100,000 edges of the DUT TX_TCLK and the link partner TX_TCLK signals.
2. Define reference edges for a jitter measurement as the 50% threshold crossing times of the MASTER (link-partner) TX_TCLK signal.
3. Define a jitter quantity, measured for each rising edge of DUT TX_TCLK signal, as the time difference between the 50% crossing of the TX_TCLK signal to the time of its corresponding reference edge. The jitter result for each rising edge on DUT TX_TCLK signal is added to a jitter histogram.
4. Compute a jitter waveform of the simultaneously captured MASTER (link partner) TX_TCLK signal relative to an *unjittered reference*.
5. Filter this jitter waveform with a 5 kHz high-pass filter to produce filtered jitter waveform JLP-TX-TCLK-MASTER-5K.
6. Ensure that the worst case SLAVE mode JTxOut (over all pairs) plus J-DUT-TX-TCLK-SLAVE-32K minus J-LP-TX-TCLK-MASTER-5K is less than 0.4 ns.

Jitter Tests Without TX_TCLK

Not all DUT provide access to TX_TCLK. Hence, in the case where your DUT does not provide access to TX_TCLK, it might be possible to perform an alternative and simpler version of the full jitter test procedure which could present some helpful information for the tests under this section.

The test procedures were published by University Of New Hampshire InterOperability Lab and can be found from their “Gigabit Ethernet Consortium Clause 40 PMA Test Suite”, version 2.4. According to the document, this procedure was yet to include in IEEE 802.3-2008 because it states “the procedure deviates from the specifications outlined in Clause 40.6.1.2.5, it is not intended to serve as a legitimate substitute for the clause...”. Thus, the following tests, based on this document, are rather as informal tests that the reported results are acted as extra information for users. For your information, all of the four jitter tests without the exposure of TX_TCLK are single clock jitter measurements.

Jitter Tests Without TX_TCLK, DUT in MASTER Mode

The formal MASTER jitter test procedure in Clause 40.6.1.2.5 of IEEE 802.3-2008 stated that JTxOut has to be measured before running the filtered jitter test as the result of the filtered jitter test is the summation of the filtered TX_TCLK jitter plus the unfiltered JTxOut. This test does not require the JTxOut measurement for the reason that it should assume JTxOut is small compared to the filtered TX_TCLK jitter in actual systems. Therefore, access to the internal TX_TCLK could become in vain when the JTxOut is assumed to be zero as the MASTER jitter at the MDI is identical to the jitter on the internal TX_TCLK.

Jitter MASTER Unfiltered Computes the unfiltered jitter on the MASTER output at the MDI relative to an unjittered reference while in the MASTER timing mode.

Jitter MASTER Filtered Computes the unfiltered jitter on the MASTER output at the MDI relative to an unjittered reference while in the MASTER timing mode and filtered by a 5 kHz high-pass filter.

NOTE For full conformance testing, unfiltered jitter measurements require 12.5 million edges. This can take up to about eight minutes per unfiltered jitter measurement. For quicker estimate of the health of a DUT, you may want to reduce the number of the unfiltered jitter edges in the “Configure” tab.

Jitter MASTER Unfiltered

The unfiltered jitter test is used to ensure that the jitter on the MASTER output at the MDI relative to the unjittered reference is less than 1.4 ns. This test will be inconclusive if the peak-to-peak result is greater than 1.4 ns.

Reference

[1] Appendix 40.B of the Gigabit Ethernet Consortium, Clause 40 PMA Test Suite Version 2.6 from University of New Hampshire InterOperability Laboratory

[2] IEEE 802.3-2008, Subclause 40.6.1.2.5

Probing Setup

NOTE When performing 1000 Base-T jitter tests for the DUT without providing access to the internal TX_TCLK, you can view the connection setup under the application's "Connection" tab (also shown in Figure 20).

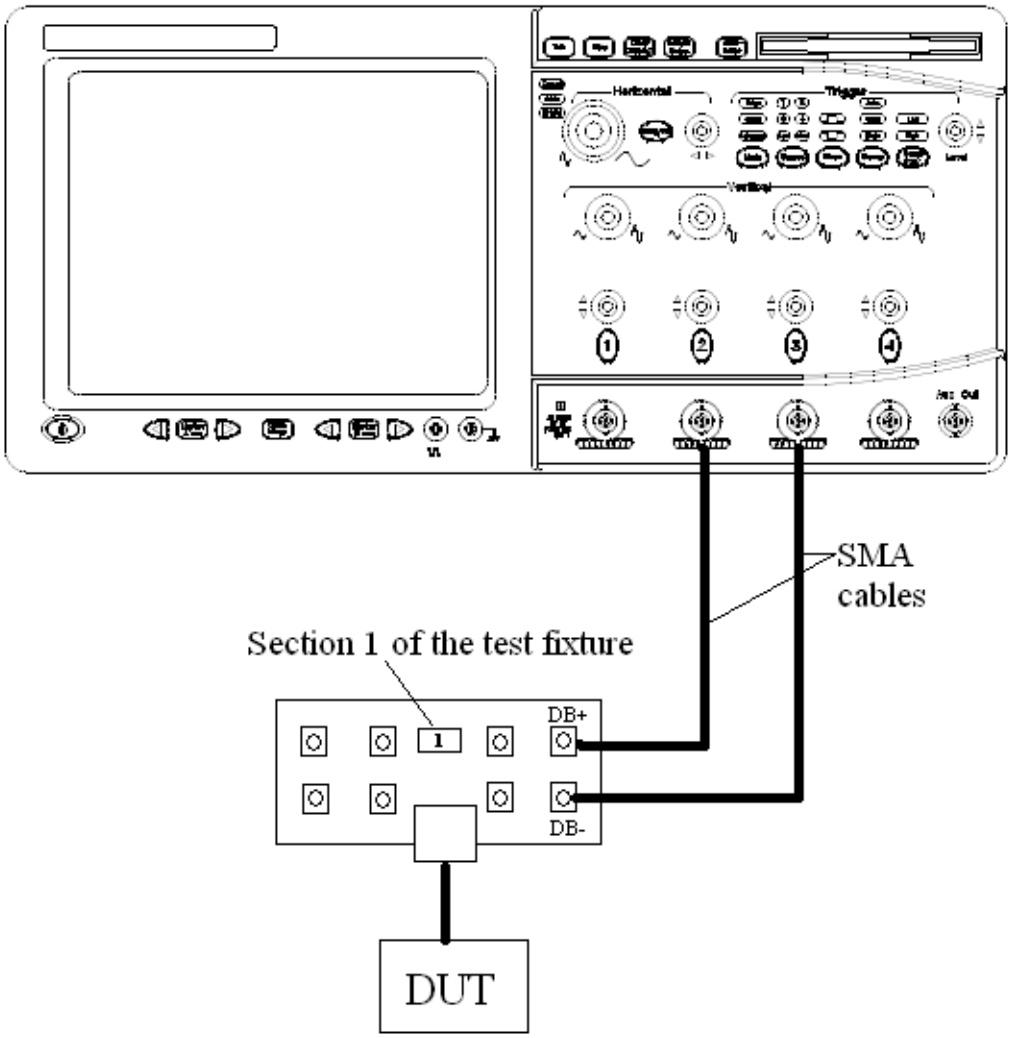


Figure 20 Probing for 1000 Base-T Jitter MASTER Unfiltered without access to TX_TCLK

1 Connect the DUT to the RJ45 connector in section 1 of the test fixture with a short straight-through UTP cable.

2 Connect one end of two short SMA-SMA cables to the SMA test points for the pair you are testing (A, B, C, or D) on fixture 1 and the other end to the Channel 3 and Channel 4 of the oscilloscope. (The channel shown in Figure 20 is just an example.)

Device Configuration

1 Configure the DUT to output the Test Mode 2 signal (MASTER timing mode).

Using your PHY vendor's provided method, set the following GMII register bits:

a Set bit 9.12 to enable MASTER-SLAVE Manual Configuration.

b Set bit 9.11 to force the DUT to become the MASTER.

c Set bit 9.15, 9.14 and bit 9.13 to the values of 0, 1, 0 to enable Test Mode 2.

2 Configure the "Dx+" to Channel 3 and "Dx-" to Channel 2.

3 Ensure that the DUT is transmitting the proper signal as indicated in the connection setup on the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signals are present on the configured "Dx+" and "Dx-" channels.
- Capture 100 ms to 1 second of the signal at MDI of the current pair.
- Compute the peak-to-peak unfiltered MASTER without TX_TCLK jitter as described in the Algorithm Discussion below, and confirm that this value is less than 1.4 ns.

NOTE

If you have selected "ALL" as the 1000 Base-T, Test Pair (under the "Configure" tab), all four pairs will be tested in sequence. You will be prompted to move the SMA cable to the test point for each test pair in turn, and this measurement will be repeated at each of these test points. If you want to debug a particular pair, select the individual pair you want to test. Note that for full compliance testing, the specification requires testing for all four pairs. At the result screen, four trial tabs are shown at the bottom left of the screen. Each trial tab contains the Test Pair BI_DB result and so on.

Algorithm Discussion

Since the DUT is not providing access to TX_TCLK and the MASTER jitter at MDI is identical to the jitter on the internal TX_TCLK, it is reasonable to measure the peak-to-peak jitter at MDI.

In the formal jitter test procedures [2], an unfiltered jitter which measures on the TX_TCLK relative to an unjittered reference must be less than 1.4 ns. For this case, the measurement is also valid to apply the same conformance limit as this test is more difficult to pass because the signal on MDI includes JTxOut. Yet, it is not possible to decide whether this test has passed or failed if the results are greater than 1.4 ns as the value of JTxOut is an unknown variable and hence, the measurement result is reported for informative purpose only.

The method to compute the unjittered reference is the same as described previously in this document.

Reference [2] states that unfiltered jitter measurements shall be made in between 100 ms and 1 second. This corresponds to 12.5 million clock periods.

As indicated in Figure 20, only the MDI data signal is connected to the oscilloscope. The algorithm proceeds as follows:

1 Capture a long record of the signal at MDI.

2 Compute ideal clock instants as discussed in the previous section.

3 Define a jitter quantity for each measured timing instant of the signal at MDI as the deviation of the 50% crossing of the signal to its corresponding ideal clock edge.

4 The jitter value for each edge on the signal at MDI is added to a jitter histogram for visualization purposes.

5 Steps 1 to 4 are repeated to acquire new data and accumulate the jitter histogram with each new acquisition until at least 100 ms of data has been analyzed.

6 The peak-to-peak value over the entire multi-acquisition jitter population is recorded as the unfiltered MASTER without TX_TCLK jitter.

Jitter MASTER Filtered

The filtered jitter test is used to ensure that the jitter on the MASTER output at the MDI relative to the unjittered reference fails if the result is greater than 0.3 ns. This test will be inconclusive if the peak-to-peak result is less than 0.3 ns.

Reference

[1] Appendix 40.B of the Gigabit Ethernet Consortium, Clause 40 PMA Test Suite Version 2.6 from University of New Hampshire InterOperability Laboratory

[2] IEEE 802.3-2008, Subclause 40.6.1.2.5

Probing Setup

Same as for Jitter MASTER Unfiltered, see “Probing Setup" on page 79.

Device Configuration

Same as for Jitter MASTER Unfiltered, see “Device Configuration" on page 80.

Performing the Test

1. Ensure this test is checked to run in the "Select Tests" tab.
2. Press the "Run Tests" button in the task flow to start testing.
3. If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.
4. The test will:
   - Verify that the correct test signal is present on the configured "Dx+" and "Dx-" channels.
   - Capture at least 100,000 edges of the signal at MDI.
     - Compute a user-configurable jitter waveform of the signal at MDI relative to an unjittered reference as described on the algorithm discussion for Unfiltered MASTER Jitter without access to TX_TCLK.
   - Filter the jitter waveform with a 5 kHz high-pass filter.
     - Compute the peak-to-peak value of the filter jitter waveform.
   - Confirm that the 5 kHz-filtered MDI data MASTER jitter fails if the result is greater than 0.3 ns.

Algorithm Discussion

This section discusses algorithms for measuring the filtered MDI data MASTER Mode jitter. In reference [2], the unfiltered JTxOut (it is the jitter between DUT TX_TCLK and the MDI data signal) is added into the filtered Master jitter test. But for the method proposed in reference [1], the JTxOut is being filtered together with the signal at MDI. Hence, this test should be easier to pass compared to the test stated in reference [2]. Thus, if the DUT produces a value greater than 0.3 ns, we can say that the test has failed.

Remember that the results obtained using this approach are inconclusive when the peak-to-peak jitter is less than 0.3 ns. By applying the same logic mentioned in unfiltered jitter case without access to TX_TCLK, it is

not possible to know how much of this value is contributed by JTxOut, unlike the formal test which measures the JTxOut prior being added to the filtered TX_TCLK MASTER Mode jitter that is exposed to TX_TCLK.

The measurement for this test is separated into two parts. The first part is to compute the jitter waveform of the MDI data signal relative to an unjittered reference which is the same as mentioned in Jitter MASTER Unfiltered without TX_TCLK. Then, filter the unfiltered jitter waveform with a 5 kHz high-pass filter.

Reference [1] states that all peak-to-peak filtered jitter measurements shall be made over an unbiased sample of at least 100,000 clock edges.

As indicated in Figure 20, only the signal at MDI is connected to the oscilloscope. The algorithm proceeds as follows:

1 Capture at least 100,000 edges of the signal at MDI in a long record.

2 Compute the jitter waveform of the signal at MDI relative to an unjittered reference as described in “Algorithm Discussion" on page 81.

3 Filter this jitter waveform with a 5 kHz high-pass filter to produce a filtered MASTER jitter waveform.

4 The jitter value for each edge on the signal at MDI is added to a jitter histogram for visualization purposes.

5 The peak-to-peak value over the entire multi-acquisition jitter population is recorded as the filtered MASTER without TX_TCLK_5K jitter.

Jitter Tests Without TX_TCLK, DUT in SLAVE Mode

Since the formal procedure for 1000Base-T SLAVE jitter is implemented to conduct the test using two DUTs operating normally and connecting to each other through their MDI ports, it has become a barrier for [1] to gain access to the internal TX_TCLK merely through MDI on fixture 1. Apart from that, a SLAVE DUT needs a PHY to provide a signal at the MDI and uses it to recover the TX_TCLK which is not possible to measure the jitter at the SLAVE's output due to the fact that each MDI wire pair is bi-directional. Thus, this section assumes that a DUT with one MDI port is put in the SLAVE timing mode and recovers its own MASTER clock which then generates the Test Mode 3 signal that complies with the standard in Clause 40.6.1.1.2.

There are two significant differences between the formal test in reference [2] and the proposed procedure in reference [1]. Firstly, it is not feasible to insert the jitter test channel between the source clock and the recovered clock in reference [1]. Secondly, when the DUT is operated in MASTER mode of the formal procedure, the jitter between the TX_TCLK and the source is also fed into the jitter test channel. However, both of these differences cause the DUT to recover a clock more easily and hence, the same SLAVE mode conformance limits cannot be applied. Because of that, the procedures suggested below are not perfect enough to judge these tests on a pass/fail basis but rather report as informative purposes only.

The following jitter tests are performed for 1000Base-T without gaining access to TX_TCLK with the DUT in SLAVE mode:

Prerequisite Compute the unfiltered jitter on the MASTER output at = MDI relative to an unjittered reference, filter with a 5 kHz high-pass filter while in the MASTER timing mode, and record both unfiltered and filtered peak-to-peak values as unfiltered MASTER without TX_TCLK jitter and filtered MASTER without TX_TCLK_5K jitter respectively.

Jitter SLAVE Unfiltered Compute the unfiltered jitter on the SLAVE output at MDI relative to an unjittered reference and record as unfiltered SLAVE. Subtract unfiltered SLAVE with unfiltered MASTER without TX_TCLK jitter.

Jitter SLAVE Filtered Filter the unfiltered SLAVE jitter by a 32 kHz high-pass filter and record as unfiltered SLAVE_32K. Subtract unfiltered SLAVE_32K with filtered MASTER without TX_TCLK_5K jitter.

NOTE Before starting the test, make sure you have already run the MASTER jitter test on the wire pair that you want to measure slave jitter. This is because the two results from the MASTER jitter test without access to TX_TCLK are needed for the following tests.

Jitter SLAVE Unfiltered

The unfiltered jitter test is used to compute the jitter on the SLAVE output at MDI relative to the unjittered reference. The result is reported for informative purpose only.

Reference

[1] Appendix 40.B of the Gigabit Ethernet Consortium, Clause 40 PMA Test Suite Version 2.6 from University of New Hampshire InterOperability Laboratory

[2] IEEE 802.3-2008, Subclause 40.6.1.2.5

Probing Setup

Same as for Jitter MASTER Unfiltered, see “Probing Setup" on page 79.

Device Configuration

1 Configure the DUT to output the Test Mode 3 signal (SLAVE timing mode).
Using your PHY vendor’s provided method, set the following GMII register bits:
   - Set bit 9.12 to enable MASTER-SLAVE Manual Configuration.
   - Clear bit 9.11 to force the DUT to become the SLAVE.
   - Set bit 9.15, 9.14 and bit 9.13 to values 0, 1, 1 respectively to enable Test Mode 3.

2 Configure the "Dx+" to Channel 3 and "Dx-" to Channel 2.

3 Ensure that the DUT is transmitting the proper signal as indicated in the connection setup on the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:
   - Verify that the Jitter MASTER unfiltered test has been run and the results recorded as unfiltered MASTER without TX_TCLK jitter.

- Verify that the correct test signals are present on the configured "Dx+" and "Dx-" channels.
- Configure the oscilloscope and capture 100 ms to 1 second of the SLAVE signal at MDI of the current pair.
- Compute the jitter waveform of the signal at MDI relative to an unjittered reference as described in “Algorithm Discussion" on page 81.
- Record the unfiltered jitter as unfiltered SLAVE.
- Subtract unfiltered SLAVE with unfiltered MASTER without TX_TCLK jitter.

NOTE If you have selected “ALL” as the 1000 Base-T, Test Pair (under the “Configure” tab), all four pairs will be tested in sequence. You will be prompted to move the SMA cable to the test point for each test pair in turn, and this measurement will be repeated at each of these test points. If you want to debug a particular pair, select the individual pair you want to test. Note that for full compliance testing, the specification requires testing for all four pairs. At the result screen, four trial tabs are shown at the bottom left of the screen. Each trial tab contains the Test Pair BI_DB result and so on.

Algorithm Discussion

This section discusses the algorithm for measuring the unfiltered SLAVE mode jitter without access to the TX_TCLK of the DUT. This test is carried out while the DUT is operating in the SLAVE timing mode without the existence of a link partner or jitter test channel which simplifies the test procedures compared to the formal Jitter SLAVE step. The only requirement for the test proposed in reference [2] is this test must only be done after the Jitter MASTER unfiltered without TX_TCLK test has been run on the wire pair which you are concerned.

Reference [2] states that unfiltered jitter measurements shall be made in between 100 ms and 1 second. This corresponds to 12.5 million clock periods.

After running the Jitter MASTER unfiltered test, we compute another jitter waveform from the captured SLAVE signal at MDI. This jitter waveform is also computed relative to an unjittered reference and the result is named as unfiltered SLAVE. Next, the unfiltered SLAVE is subtracted with unfiltered MASTER without TX_TCLK jitter and the unfiltered SLAVE jitter waveform is produced as unfiltered SLAVE without TX_TCLK jitter.

The test neither passes nor fails because there is no conformance limit that can be applied yet.

As indicated in Figure 20, only the signal at MDI is connected to the oscilloscope. The algorithm proceeds as follows:

1 Verify if the Jitter MASTER filtered test has been run prior to this test.

2 Capture a long record of the signal at MDI.

3 Compute ideal clock instants as discussed in the previous section.

4 Define a jitter quantity for each measured timing instant of the signal at MDI as the deviation of the 50% crossing of the signal to its corresponding ideal clock edge.

5 Compute the unfiltered jitter on the SLAVE output at MDI relative to an unjittered reference and record as unfiltered SLAVE.

6 Subtract unfiltered SLAVE with unfiltered MASTER without TX_TCLK jitter.

7 Steps 1 to 4 are repeated to acquire new data and accumulate the jitter histogram with each new acquisition until at least 100 ms of data has been analyzed.

8 The peak-to-peak value over the entire multi-acquisition jitter population is recorded as the unfiltered SLAVE without TX_TCLK jitter.

Jitter SLAVE Filtered

The filtered jitter test is used to compute the jitter on the SLAVE output at MDI relative to the unjittered reference, filter the jitter waveform with a 32 kHz high-pass filter and measure the peak-to-peak jitter value called filtered SLAVE_32K. Then, subtract the filtered SLAVE_32K with the filtered MASTER without TX_TCLK_5K jitter. The result is reported for informative purpose only.

Reference

[1] Appendix 40.B of the Gigabit Ethernet Consortium, Clause 40 PMA Test Suite Version 2.6 from University of New Hampshire InterOperability Laboratory

[2] IEEE 802.3-2008, Subclause 40.6.1.2.5

Probing Setup

Same as for Jitter MASTER Unfiltered, see “Probing Setup" on page 79.

Device Configuration

Same as for Jitter SLAVE Unfiltered, see “Device Configuration" on page 86.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the Jitter MASTER filtered test has been run and the results recorded as filtered MASTER without TX_TCLK_5K jitter.
- Verify that the correct test signals are present on the configured "Dx+" and "Dx-" channels.
- Capture at least 100,000 edges of the signal at MDI in one long record.
- Compute the jitter waveform of the signal at MDI relative to an unjittered reference as described in “Algorithm Discussion" on page 81.
- Filter this jitter waveform with a 32 kHz high-pass filter then subtract the jitter waveform with filtered MASTER without TX_TCLK_5K jitter.
- Refer to the “Algorithm Discussion below for further details.

Algorithm Discussion

This section discusses the algorithm for measuring the filtered SLAVE mode jitter without access to the TX_TCLK of the DUT. This test is carried out while the DUT is operating in the SLAVE timing mode without the existence of a link partner or jitter test channel as well. The only requirement for the test proposed in reference [2] is this test must only be done after the Jitter MASTER filtered without TX_TCLK test has been run on the wire pair you are concerned with.

Reference [2] states that all peak-to-peak filtered jitter measurements shall be made over an unbiased sample of at least 100,000 edges.

Section “Jitter Slave Unfiltered without TX_TCLK” discusses the computation of an unfiltered jitter waveform of the SLAVE signal on MDI relative to the unjittered reference. We then filter this jitter waveform with a 32 kHz high-pass filter to produce a filtered jitter waveform called filtered SLAVE_32K.

We also need the filtered MASTER without TX_TCLK_5K jitter from the Jitter MASTER filtered without TX_TCLK test to subtract by the filtered SLAVE_32K and record the result as filtered SLAVE without TX_TCLK_32K jitter.

The test neither passes nor fails because there is no conformance limit yet to apply for this section.

As indicated in Figure 20, only the signal at MDI is connected to the oscilloscope. The algorithm proceeds as follows:

1 Verify if the Jitter MASTER filtered test has been run prior to this test.

2 Verify that the correct test signals are present on the configured "Dx+" and "Dx-" channels.

3 Capture at least 100,000 edges of the signal at MDI in one long record.

4 Compute the jitter waveform of the signal at MDI relative to an unjittered reference.

5 Filter this jitter waveform with a 32 kHz high-pass filter to produce a filtered SLAVE jitter waveform and record as filtered SLAVE_32K.

6 Subtract filtered SLAVE_32K with filtered MASTER without TX_TCLK_5K jitter.

7 The peak-to-peak value over the entire multi-acquisition jitter population is recorded as the filtered SLAVE without TX_TCLK_32K jitter.

MDI Return Loss

NOTE This section shows the use of a Vector Network Analyzer (VNA) used for testing MDI Return Loss. However, you can use in place of the VNA an exported VNA file in either the Touchstore or CITI file format.

This section describes the 1000 Base-T MDI return loss test as per IEEE 802.3-2008, Subclause 40.8.3.1. The test procedures described in this section cover the MDI return loss measurement required by the specification.

Reference

[1] IEEE 802.3-2008, Subclause 40.8.3.1

Calibrating the VNA

Before using the VNA, it must be calibrated using the Return Loss Calibration board. See Figure 21 for the connection diagram.

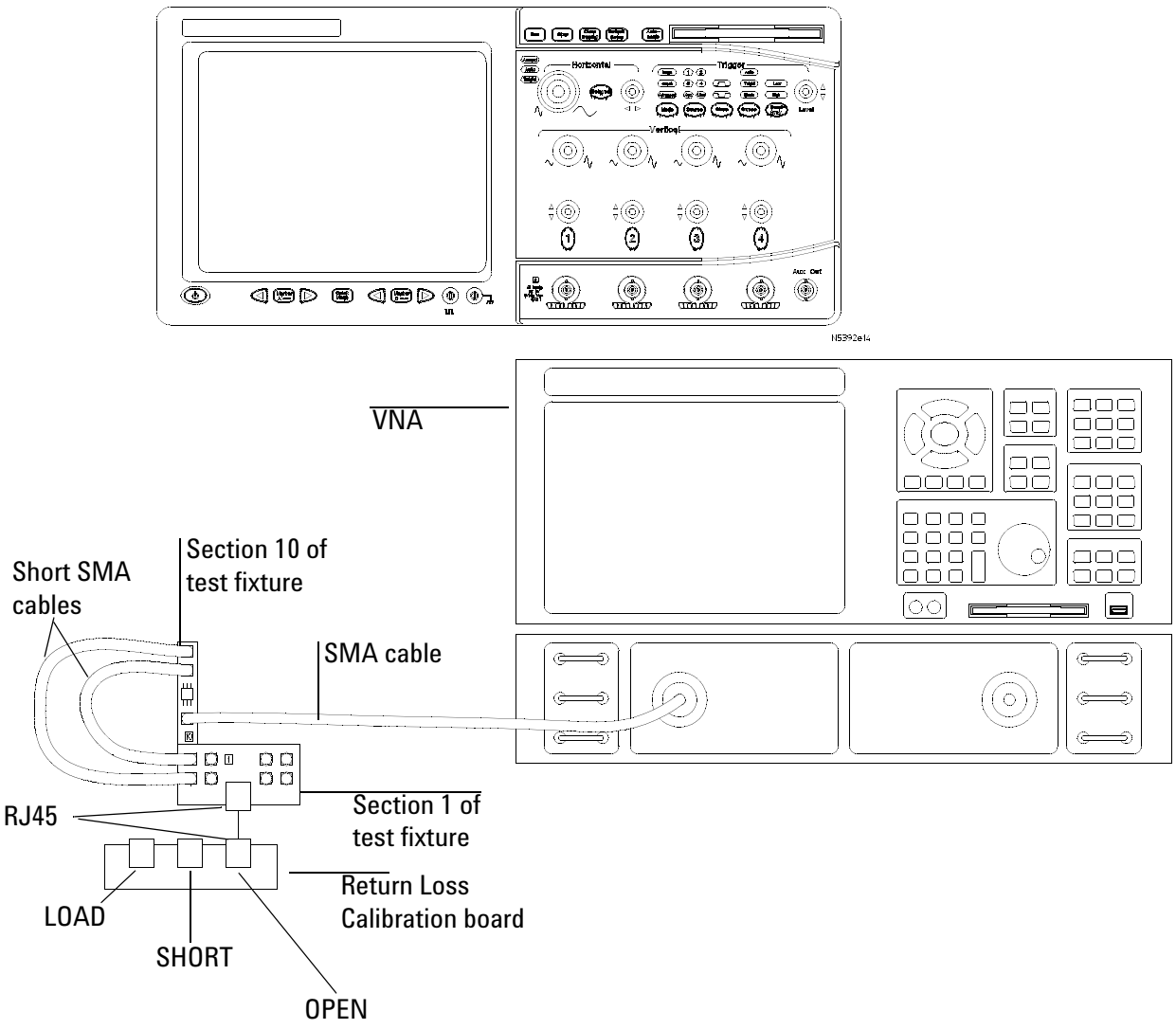


Figure 21 VNA Calibration

1 Connect the Return Loss Calibration board RJ45 connector labeled OPEN to the RJ45 connector on fixture 1 using a short straight-through UTP cable.

2 Connect one end of two short SMA-to-SMA cables to the SMA test points for the pair you are testing (A, B, C, or D) on fixture 1, and the other end to the two SMA (X97 and X98) test points on fixture 10.

3 Connect a VNA input to the SMA (X99) test point on fixture 10.

4 Calibrate the VNA using the instructions in the VNA's User's Guide. The following is a list of setup requirements.

- Set Meas to Ref1 Fwd S11.
- Set Start to 1 MHz.
- Set Stop to 100 MHz.
- Set Format to Log Mag.
- Set Scale Div to 5.
- Set Scale Ref to reference line position 9.

5 Run the calibration for the OPEN, SHORT, and LOAD connections.

Probing Setup for MDI Return Loss

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

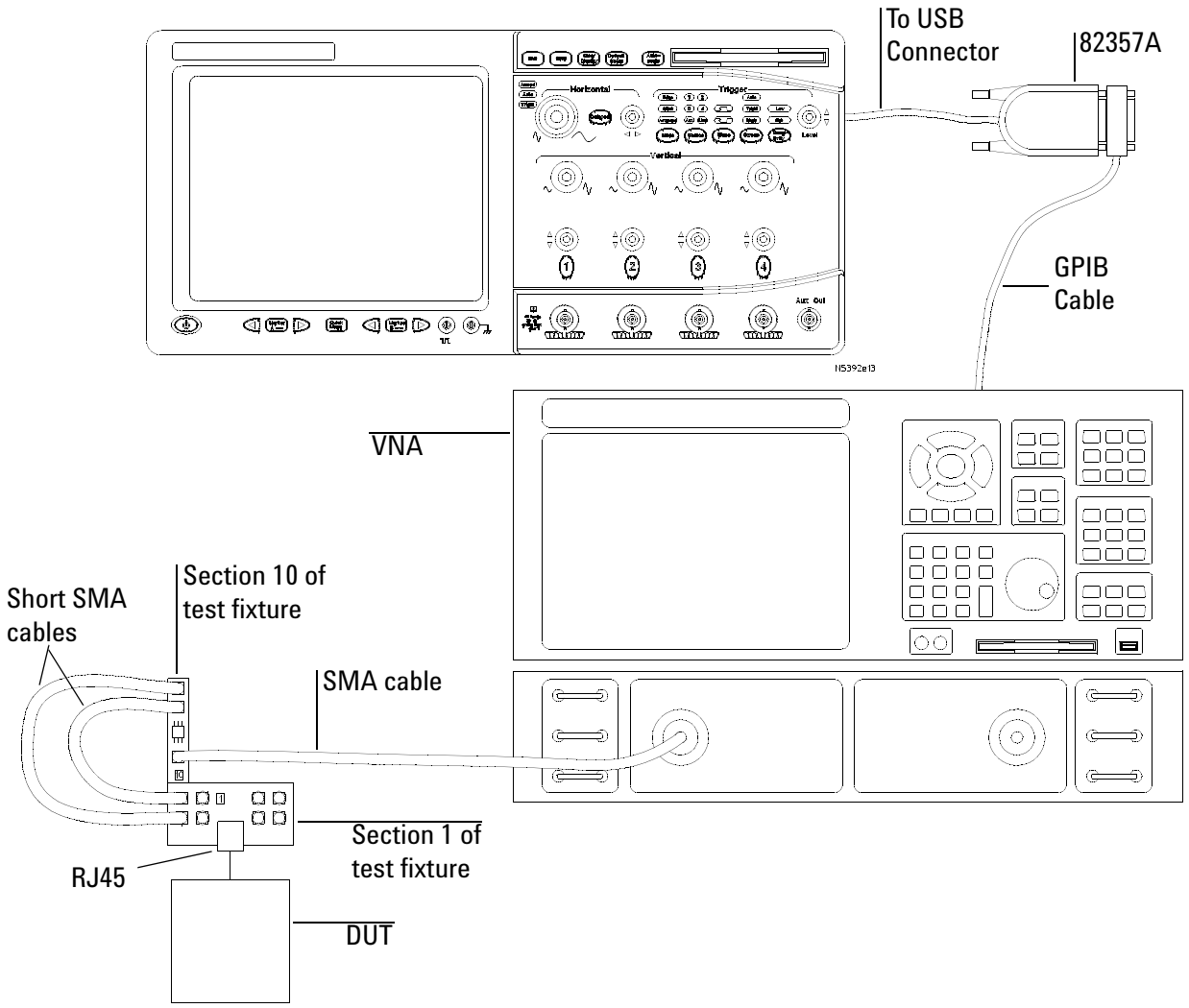


Figure 22 Probing for 1000 Base-T MDI Return Loss

1. Connect the DUT to the RJ45 connector on fixture 1 using a short straight-through UTP cable.
2. Connect one end of two short SMA-to-SMA cables to the SMA test points for the pair you are testing (A, B, C, or D) on fixture 1, and the other end to the two SMA (X97 and X98) test points on fixture 10.
3. Connect a VNA input to the SMA (X99) test point on fixture 10.

4 Connect a GPIB cable to the 82357A GPIB port and to the GPIB port on the VNA.

5 Connect the 82357A USB connector to a USB port on the scope.

Device Configuration

1 Configure the DUT to output the Test Mode 4 signal (MASTER timing mode).

Using your PHY vendor's provided method, set the DUT's GMII register bits 9.15, 9.14, 9.13 to the values 1, 0, 0 respectively.

2 Ensure that the DUT is transmitting the proper signal as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Compute the return loss as described in the Algorithm Discussion below.

NOTE If you have selected "ALL" as the 1000 Base-T, Test Pair (under the "Configure" tab), all 4 pairs will be tested in sequence. You will be prompted to move the probe to the test point for each test pair in turn, and this measurement will be repeated at each of these test points. If you want to debug a particular pair, select the individual pair you wish to test. Note that for full compliance testing, the specification requires testing all 4 pairs. At the result screen, 4 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Test Pair BI_DA result, Trial 2 contains Test Pair BI_DB result and so on.

Algorithm Discussion

Reference [1] describes all the transmit/receive channel return loss specifications for a 1000 Base-T device at the physical medium attachment (PMA) sublayer to Media Dependent Interface (MDI). The differential impedance at the MDI for each transmit/receive channel shall be such that any refection due to differential signals incident to the MDI from a balanced cabling having an impedance of 100 Ω ± 15% is attenuated, relative to the incident signal, at least 16 dB over the frequency range of

1.0 MHz to 40 MHz and at least 10 – $20\log_{10}(f/80)$ dB over the frequency range 40 MHz to 100 MHz (f in MHz). This return loss shall be maintained at all times when the PHY is transmitting data or control symbols.

5
100 Base-TX Tests

This section provides the Methods of Implementation (MOIs) for 100 Base-TX tests using an Agilent Infiniium oscilloscope, probes, and the Ethernet Compliance Test Application.

Probing for 100 Base-TX Tests

Connectivity for 100 Base-TX tests depends on whether you need a link partner to obtain the scrambled /idle/ sequence. If your device does not require a link partner, see "Probing for 100 Base-TX Tests, Without Link Partner". Otherwise, if your device does require a link partner, see "Probing for 100 Base-TX Tests, With Link Partner".

Probing for 100 Base-TX Tests, Without Link Partner

When performing the 100 Base-TX tests without a link partner, the Ethernet Compliance Test Application will prompt you to make the proper connections (also shown in Figure 23).

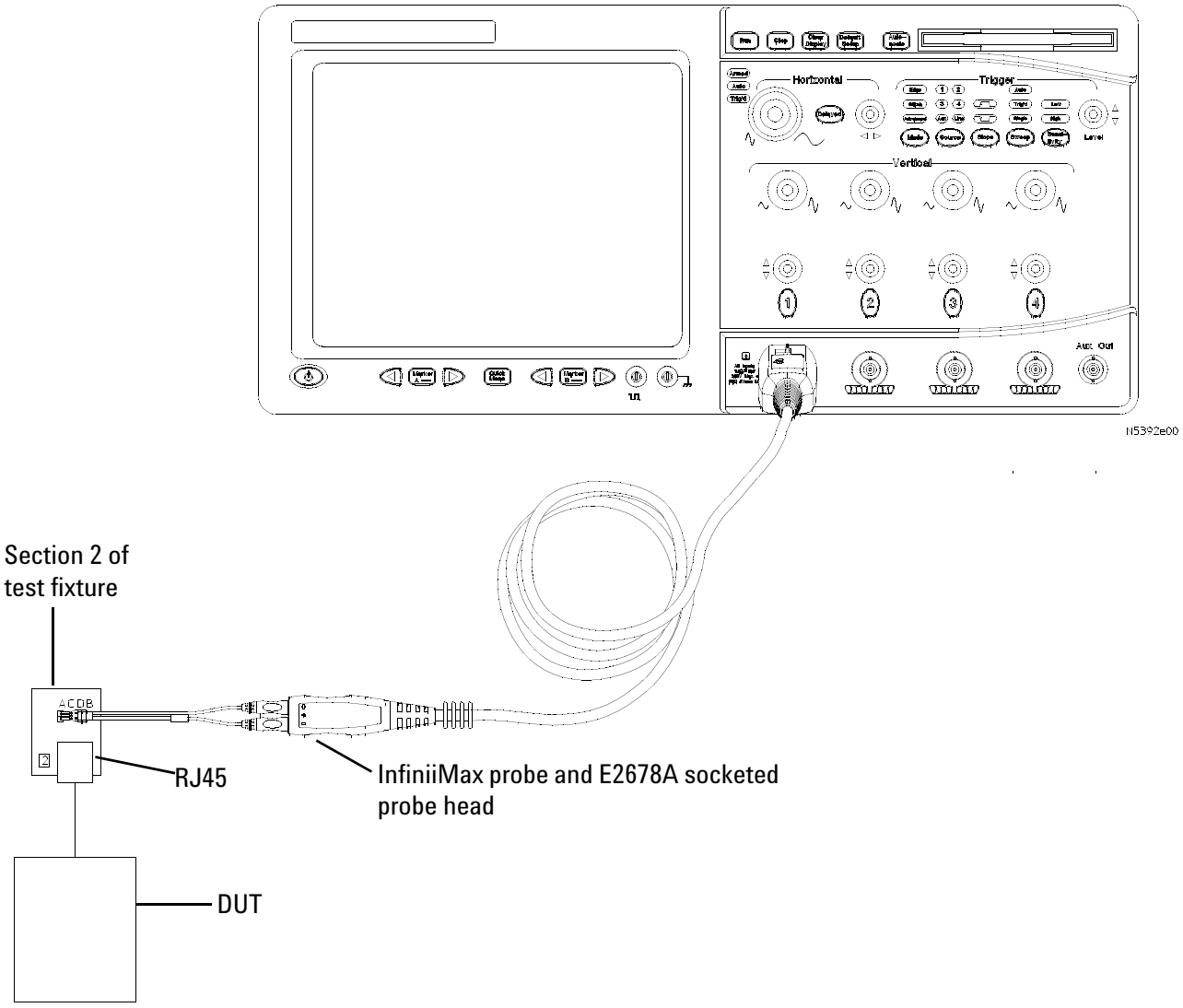


Figure 23 Probing for 100 Base-TX Tests, Without Link Partner

1 Connect the DUT to the RJ45 connector on section 2 of the Ethernet test fixture (load and probes) using a short UTP cable.

2 Connect an InfiniiMax probe with differential socketed probe head to test point TP4, and to the configured “Data” channel of the oscilloscope.

3 Ensure correct polarity of the probe head.

You can use any of the oscilloscope channels for probing the test point. You can identify the channel used in the Configure tab of the Ethernet Compliance Test Application. (The channel shown in Figure 23 is just for example.)

Probing for 100 Base-TX Tests, With Link Partner

When performing the 100 Base-TX tests with a link partner, the Ethernet Compliance Test Application will prompt you to make the proper connections (also shown in Figure 24).

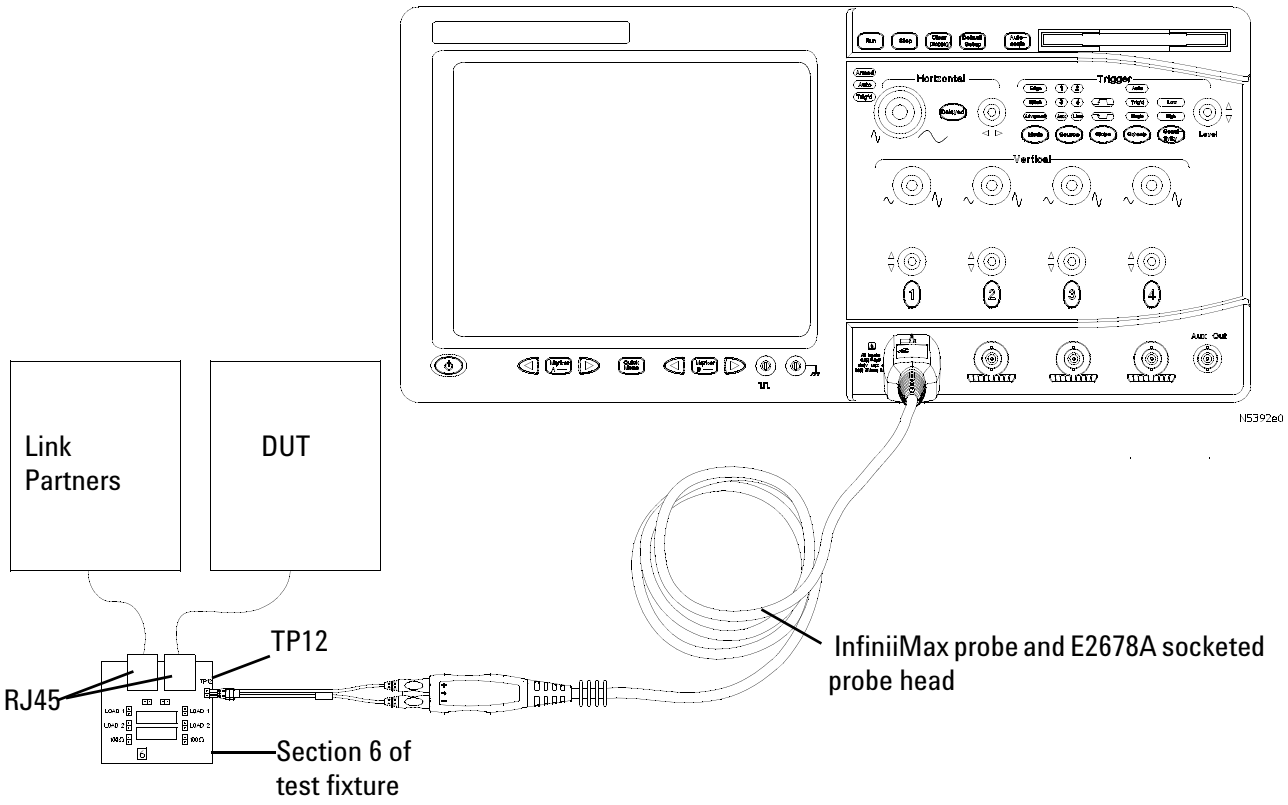


Figure 24 Probing for 100 Base-TX Tests, With Link Partner

1. Connect the DUT to the RJ45 connector on fixture 6 marked DUT (J9) using a short UTP cable.
2. Connect a 100 Base-TX link partner to the RJ45 connector on fixture 6 marked LP (J8) using a short UTP cable.
3. Connect an InfiniiMax differential probe with E2678A differential socketed probe head to TP14 and to the configured “DUT Data” channel on the oscilloscope.
4. Using two jumpers, short the 100Ω load on fixture 6.

You can use any of the oscilloscope channels for probing the test point. You can identify the channel used in the Configure tab of the Ethernet Compliance Test Application. (The channel shown in Figure 24 is just for example.)

Peak Voltage Tests

UTP +Vout Differential Output Voltage

UTP -Vout Differential Output Voltage

The UTP +/-Vout Differential Output Voltage tests are to verify that the differential output voltage of the device under test (DUT) is within the conformance limits.

References

[1] IEEE 802.3-2008, clause 25.

[2] ANSI X3.263-1995, Section 9.1.2.2.

Probing Setup

Refer to "Probing for 100 Base-TX Tests" on page 98. This probing configuration is used for all 100 Base-TX tests.

Device Configuration

1. Configure the DUT for 100 Base-TX operation.
2. Ensure that the DUT is sending scrambled, MLT-3 encoded /I/ code-groups (this is a 3-level pseudo-random bit sequence).

Performing the Test

1. Ensure this test is checked to run in the “Select Tests” tab.
2. Press the “Run Tests” button in the task flow to start testing.
3. If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to “I have completed these instructions” near the bottom of this dialog. Then, press the “Next” button to continue testing.
4. The test will:
   - Verify that the correct test signal is present on the configured Data channel.
   - Configure the oscilloscope to capture a 96 ns pulse.
   - Test the signal against conformance parameters, recording the result.

Algorithm Discussion

Reference [1] describes the operation of the Physical Medium Dependent (PMD) sublayer for 100 Base-TX devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the differential output voltage at the Active Output Interface (AOI) for operation over unshielded twisted pair (UTP).

The reference for this measurement is defined by the standard as an output waveform consisting of 14 bit times of no transition preceded by a transition from 0 V to Vout. This reference waveform was chosen under the assumption that the DUT would be sending scrambled, MLT-3 encoded /H/ code-groups. While this is normal for an FDDI device, it is not straightforward to get a 100 Base-TX device to generate this sequence. A 100 Base-TX device normally generates scrambled, MLT-3 encoded /I/ code-groups in which one may find 12 bit times (96 ns) of no transition preceded by a transition from 0 V to Vout. Thus, a 96 ns pulse is used as the reference for our measurement.

This algorithm measures Vout as the mean voltage over the time range defined in Figure 25. This time range extends from 8 ns after the signal rise crosses 50% of Vout to 8 ns before the signal fall crosses 50% of Vout. The figure depicts +Vout. A similar measurement is made for -Vout considering the negative going pulse.

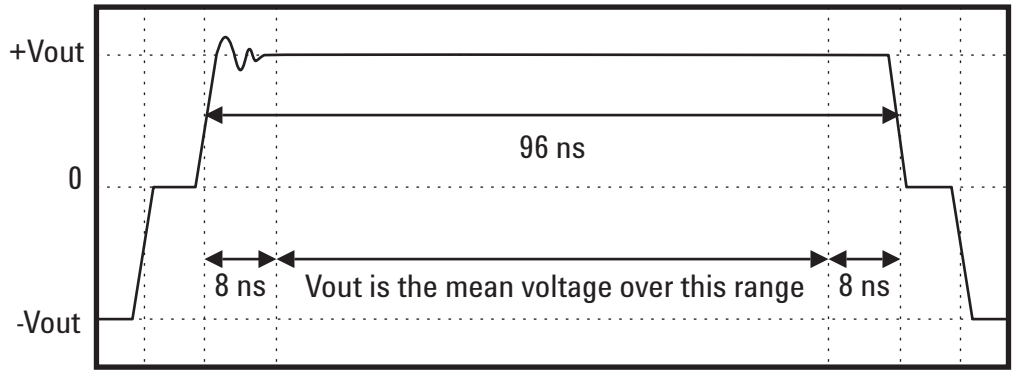


Figure 25 Mean Voltage Over the Time Range

In compliance mode, averaging is used for enhanced accuracy. Note that other 100 Base-TX measurements depend on the accurate measurement of Vout.

Signal Amplitude Symmetry

The Signal Amplitude Symmetry test is to verify that the differential output signal amplitude symmetry of the device under test (DUT) is within the conformance limits.

References

[1] IEEE 802.3-2008, clause 25.

[2] ANSI X3.263-1995, Section 9.1.2.2.

Probing Setup

Refer to "Probing for 100 Base-TX Tests" on page 98. This probing configuration is used for all 100 Base-TX tests.

Device Under Test Configuration

1. Configure the DUT for 100 Base-TX operation.
2. Ensure that the DUT is sending scrambled, MLT-3 encoded /I/ code-groups (this is a 3-level pseudo-random bit sequence).

Performing the Test

1. Ensure this test is checked to run in the "Select Tests" tab.
2. Press the "Run Tests" button in the task flow to start testing.
3. If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then press the "Next" button to continue testing.
4. The test computes its results entirely from the results of the following prerequisite tests:
   - UTP +Vout Differential Output Voltage.
   - UTP -Vout Differential Output Voltage.
5. If the prerequisite tests have not yet been run, they are first run.
6. The test will compute the symmetry as follows:

   Symmetry = | +Vout/ -Vout |

   The allowable range is 0.88 to 1.0.

NOTE The specified constraints for this measurement are extremely tight. If this test fails, please consult the vertical gain specifications for your oscilloscope before drawing any conclusions about conformance.

Overshoot Tests

+Vout Overshoot

-Vout Overshoot

The UTP +/-Vout Differential Output Voltage tests are to verify that the waveform overshoot of the device under test (DUT) is within the conformance limits.

References

[1] IEEE 802.3-2008, clause 25.

[2] ANSI X3.263-1995, Section 9.1.3.

Probing Setup

Refer to "Probing for 100 Base-TX Tests" on page 98. This probing configuration is used for all 100 Base-TX tests.

Device Configuration

1 Configure the DUT for 100 Base-TX operation.

2 Ensure that the DUT is sending scrambled, MLT-3 encoded /I/ code-groups (this is a 3-level pseudo-random bit sequence).

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel.
- Configure the oscilloscope to capture a 96 ns pulse.
- Compute the waveform overshoot as described in the Algorithm Discussion below, compare this value against conformance parameters, recording the result.

Algorithm Discussion

Reference [1] describes the operation of the Physical Medium Dependent (PMD) sublayer for 100 Base-TX devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the waveform overshoot at the Active Output Interface (AOI).

The specification does not define a reference waveform for this measurement. We adopt the same reference waveform used in +/-Vout Differential Output voltage waveforms (a 96 ns pulse). See "Peak Voltage Tests" on page 102.

Waveform overshoot is defined as the relative percentage of the worst excursion of the signal transition beyond its final adjusted value. Accurately determining the end of the signal transition may be difficult.

This algorithm determines the waveform overshoot as follows:

- Measure the peak voltage over the waveform from the time of the 50% crossing point to a time 8 ns after this point. Define this worst excursion as Vpeak.
- Compute the waveform overshoot as (Vpeak - Vout)/Vout * 100%.
- Note that this measurement requires the Vout measurement (a separate test).

The waveform overshoot must be less than 5%. Waveform overshoot is computed using the above method for both positive going and negative going transitions. In compliance mode, averaging is used to reduce measurement noise and increase measurement resolution.

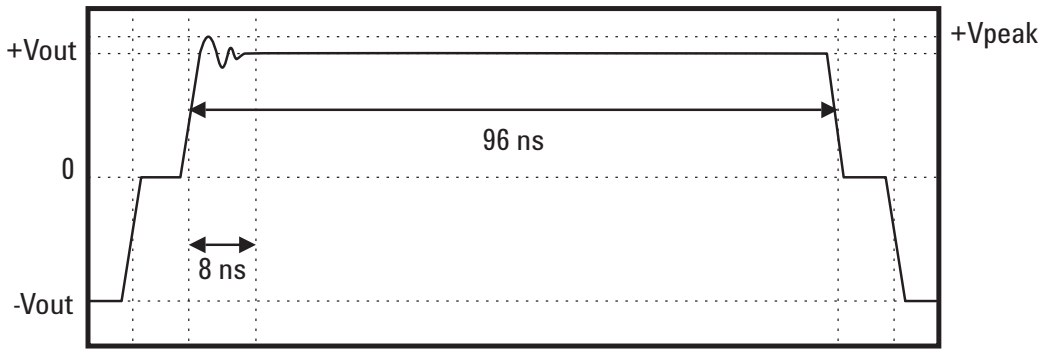


Figure 26 Waveform Overshoot Reference Waveform

Template Tests

UTP AOI Template

The UTP AOI Template test is provided for informative purposes. The specification does not require that this test be run, but it may be useful in providing insight of potential signal quality issues.

References

[1] IEEE 802.3-2008, clause 25.

[2] ANSI X3.263-1995, Annex J.

Probing Setup

Refer to "Probing for 100 Base-TX Tests" on page 98. This probing configuration is used for all 100 Base-TX tests.

Device Configuration

1. Configure the DUT for 100 Base-TX operation.
2. Ensure that the DUT is sending scrambled, MLT-3 encoded /I/ code-groups (this is a 3-level pseudo-random bit sequence).

Performing the Test

1. Ensure this test is checked to run in the "Select Tests" tab.
2. Press the "Run Tests" button in the task flow to start testing.
3. If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.
4. The test will:
   - Verify that the correct test signal is present on the configured "DUT Data" channel.
   - Configures the oscilloscope to trigger the signal.
   - Automatically aligns the mask to the waveform as indicated in the Algorithm Discussion.

NOTE If alignment fails you can either retry automatic alignment or go to the oscilloscope and manually align the mask to the signal before pressing "Next" to continue.

- Window the signal in order to test the top part of the mask.
- Acquire a number of waveforms as configured by the user, testing each waveform against the mask. The total number of failures on the top part of the mask is recorded.
- Window the signal in order to test the bottom part of the mask.
- Acquire a number of waveforms as configured by the user, testing each waveform against the mask. The total number of failures on the bottom part of the mask is recorded.
- The total number of failures (top + bottom) is recorded.

Algorithm Discussion

Reference [1] describes the operation of the Physical Medium Dependent (PMD) sublayer for 100 Base-TX devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the informative only AOI Template test at the Active Output Interface (AOI).

The specification does not require this test. It is provided for informative purposes. The template in Figure J.1 of Reference[2] is first centered vertically on the eye pattern baseline. It is then translated horizontally and scaled in amplitude for the best fit to the eye pattern. The scaling range is limited to the range specified in Reference[2] (0.95 and 1.05 for UTP).

Once the mask is aligned to the signal, the software analyzes the top portion of the mask. This reduces the contribution of vertical noise error to the measurement. The application acquires a configurable number of waveforms. Each waveform is tested against the mask. The total number of failures for the top half of the mask is recorded.

The above procedure is repeated for the bottom half of the mask, recording the number of failures for the bottom as well. The total number of failures is reported. Ideally, the total number of failures should be zero, though this is not a requirement for conformance.

Rise and Fall Time Tests

This section deals with all the 100 Base-TX Rise and Fall time measurements. The following tests are covered:

AOI +Vout Rise Time

AOI +Vout Fall Time

AOI +Vout Rise/Fall Symmetry

AOI -Vout Rise Time

AOI -Vout Fall Time

AOI -Vout Rise/Fall Symmetry

AOI Overall Rise/Fall Symmetry

Test Purpose

Table 18 100 Base-TX Rise and Fall time Tests

Test	Purpose
AOI +Vout Rise Time	To verify that the signal rise of the positive pulse (0 to +Vout) of the device under test (DUT) is within the conformance limits (3 to 5 ns).
AOI +Vout Fall Time	To verify that the signal fall of the positive pulse (+Vout to 0) of the device under test (DUT) is within the conformance limits (3 to 5 ns).
AOI +Vout Rise/Fall Symmetry	To verify that the difference between all measured rise and fall times of the positive pulse (+Vout) of the device under test (DUT) is within the conformance limits (500 ps).
AOI -Vout Rise Time	To verify that the signal rise of the negative pulse (0 to -Vout) of the device under test (DUT) is within the conformance limits (3 to 5 ns).
AOI -Vout Fall Time	To verify that the signal fall of the negative pulse (-Vout to 0) of the device under test (DUT) is within the conformance limits (3 to 5 ns).
AOI -Vout Rise/Fall Symmetry	To verify that the difference between all measured rise and fall times of the positive pulse (+Vout) of the device under test (DUT) is within the conformance limits (500 ps).

Table 18 100 Base-TX Rise and Fall time Tests

Test	Purpose
AOI Overall Rise/Fall Symmetry	To verify that the difference between the maximum and minimum value from all the measured rise and fall times of the positive pulse (+Vout) and negative pulse (-Vout) of the device under test (DUT) is within the conformance limits (500 ps).

References

[1] IEEE 802.3-2008, clause 25.

[2] ANSI X3.263-1995, Subclause 9.1.6.

Probing Setup

Refer to "Probing for 100 Base-TX Tests" on page 98. This probing configuration is used for all 100 Base-TX tests.

Device Configuration

1 Configure the DUT for 100 Base-TX operation.

2 Ensure that the DUT is sending scrambled, MLT-3 encoded /I/ code-groups (this is a 3-level pseudo-random bit sequence).

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel.
- Configure the oscilloscope to capture a 96 ns pulse.
- Compute the waveform overshoot as described in the Algorithm Discussion below, compare this value against conformance parameters, recording the result.

Algorithm Discussion

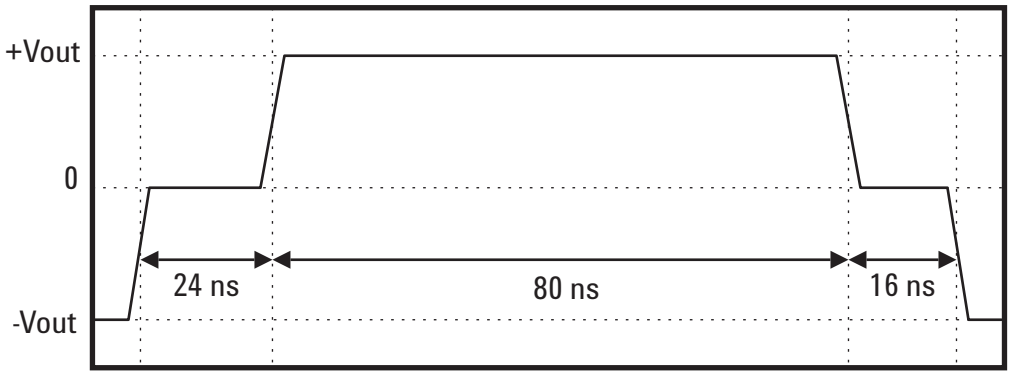


Figure 27 Rise and Falltime Reference Waveform

DCD/Jitter Tests

Transmit Jitter

The 100 Base-TX Transmit Jitter test ensures that the total transmit jitter of the signal at the Active Output Interface (AOI) is within conformance limits.

References

[1] IEEE 802.3-2008, clause 25.

[2] ANSI X3.263-1995, Subclause 9.1.9.

Probing Setup

Refer to "Probing for 100 Base-TX Tests" on page 98. This probing configuration is used for all 100 Base-TX tests.

Device Configuration

1 Configure the DUT for 100 Base-TX operation.

2 Ensure that the device is sending scrambled, MLT-3 encoded /I/ code-groups (this is a 3-level pseudo-random bit sequence).

NOTE

You can also have the device send scrambled, MLT-3 encoded /H/ code-groups for this test.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel.
- Configure the oscilloscope to capture the waveform.
- Use a software implemented 125 MHz PLL to recover the clock from the data, and synchronize the oscilloscope to the recovered clock.

- The application acquires a number of waveforms to achieve the user-configurable total number of UI. Note that the number of actual crossings measured will be less than the total number of UI acquired, because not every UI results in a crossing at the threshold.
- Window the signal to the top crossing. Acquire half of the total requested UI, measuring the width of the top crossing.
- Window the signal to the bottom crossing. Acquire half of the total requested UI, measuring the width of the bottom crossing.
- Compute the peak-to-peak jitter as the maximum width crossing (top or bottom).

Algorithm Discussion

Reference [1] describes the operation of the Physical Medium Dependent (PMD) sublayer for 100 Base-TX devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the total transmit jitter at the Active Output Interface (AOI).

Reference[2] indicates that the measurement should be performed on scrambled, MLT-3 encoded /H/ code-groups. Reference [1] which supersedes the ANSI specification states that this measurement may alternatively be made on scrambled, MLT-3 encoded /I/ code-groups.

Note that the specification does not provide any requirements or suggestions as to the population over which to compute total jitter, or the BER at which to measure jitter. Because jitter is a statistical phenomenon, with some random components, measuring jitter over a larger population will provide increasingly larger peak-to-peak values (the tails of a Gaussian distribution are infinitely long).

In general, in order to accurately determine peak-to-peak jitter, we recommend that the jitter be measured over 100M UI. This corresponds to a BER of 10^8. However, measuring jitter over such a large population is often impractical. The user can configure the number of UI over which to measure jitter in the Configure tab of the application. The default value of 100,000 UI is a trade off of statistical confidence for runtime efficiency. However, the user may wish to run this measurement over a smaller population, to decrease runtime, or a larger population, to increase statistical confidence.

The specification does not provide any specific constraints on the size of the jitter population or statistical confidence of the measurement.

It is clear from Reference [2] that the jitter measurement should include contributions from duty cycle distortion and baseline wander. Note that there are two crossing (top and bottom) at which we must measure jitter. While the specification provides no explicit instructions for choosing thresholds, we must choose voltage thresholds at which to measure the crossing points.

Figure 14 of Subclause 9.1.8 of the ANSI specification clearly defines the positive 50% crossing threshold as +Vout/2. However, the specification does not clearly indicate whether the bottom threshold should be -(+Vout/2) or (-Vout)/2. Because this measurement is to include the effects of duty cycle distortion and baseline wander, we choose the bottom threshold as -(+Vout/2).

Figure 28 illustrates the effects of choosing -(+Vout/2) as the bottom crossing threshold. The reference waveform is redrawn with exaggerated baseline wander. Note that the choice of -(+Vout/2) as the bottom threshold results in worse duty cycle distortion value than if -Vout/2 were chosen as the negative threshold.

Jitter is measured as the deviation of measured timing instants from an ideal timing reference. It is not clear from the specification whether the transmit clock or a recovered clock is to be used for a timing reference. To simplify the test setup, we assume the recovered clock as the timing reference for jitter. The recovered clock is derived from the data signal by applying the software equivalent of a 125 MHz phase locked loop (PLL) phase locked to the data signal.

The application windows the signal at the top crossing point and bottom crossing point in two steps. This is done in order to minimize the effects of vertical noise on the measurement. Half the requested number of jitter UI are acquired at the top crossing, and the other half are acquired at the bottom crossing. The crossing widths of the top and bottom crossings are recorded, and the peak-to-peak jitter is computed as the largest of these two crossing widths. For a compliant device, the peak-to-peak jitter must not exceed 1.4 ns.

Duty Cycle Distortion

The 100 Base-TX Duty Cycle Distortion test ensures that the peak-to-peak Duty Cycle Distortion of the signal at the Active Output Interface (AOI) is within conformance limits.

References

[1] IEEE 802.3-2008, clause 25.

[2] ANSI X3.263-1995, Subclause 9.1.8.

Probing Setup

Refer to “Probing for 100 Base-TX Tests" on page 98. This probing configuration is used for all 100 Base-TX tests.

Device Configuration

1 Configure the DUT for 100 Base-TX operation.

2 Ensure that the DUT is sending the MLT-3 encoded 01010101 NRZ bit sequence as shown in Figure 28.

NOTE You may send maximum length packets with a payload of 010101...

NOTE Alternatively, you may have the device send scrambled, MLT-3 encoded /I/ code-groups (this is a 3-level pseudo-random bit sequence).

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel.
- Configure the oscilloscope to capture the waveform.
- Measure the edge times of the 4 edges t0-t3 as indicated in the Algorithm Discussion.
- Compute the edge differences as indicated in the Algorithm Discussion. Differences are computed for:
  - t1-t0 (nominally 16 ns)
  - t2-t1 (nominally 16 ns)
  - t3-t2 (nominally 16 ns)
  - t2-t0 (nominally 32 ns)
  - t3-t1 (nominally 32 ns)
  - t3-t0 (nominally 48 ns)
- Compute the worst case peak-to-peak Duty Cycle Distortion as the largest deviation from the nominal distance.

Algorithm Discussion

Reference [1] describes the operation of the Physical Medium Dependent (PMD) sublayer for 100 Base-TX devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines duty cycle distortion (DCD) at the Active Output Interface (AOI).

Reference[2] indicates a reference waveform of 4 successive MLT-3 transitions generated by the MLT-3 encoded NRZ bit sequence 01010101. We further distinguish our reference waveform as one that is preceded and followed by at least two symbols at the baseline voltage (the exact sequence chosen as the reference waveform is 000101010100). This choice of a reference waveform reduces the effects of intersymbol interference (ISI).

It is clear from Figure 14 in Reference[2] that the threshold for measuring the 50% crossing of positive-going pulses should be (+Vout)/2. Note that figure 14 in Reference [2] depicts an ideal waveform, so it is not explicitly clear whether the bottom threshold should be chosen as (-Vout)/2 or -(+Vout/2).

It is clear from clause 9.1.9 that the jitter measurement should include contributions from duty cycle distortion and baseline wander. It is therefore assumed that the duty cycle distortion measurement should include effects of baseline wander. Therefore, we choose the bottom threshold for the 50% crossing times as -(+Vout/2), that is, the negative of +Vout/2.

Figure 28 illustrates the effects of choosing -(+Vout/2) as the bottom crossing threshold. The reference waveform is redrawn with exaggerated baseline wander. Note that the choice of -(+Vout/2) as the bottom threshold causes a worst peak-to-peak duty cycle distortion value than if -Vout/2 were chosen as the negative threshold.

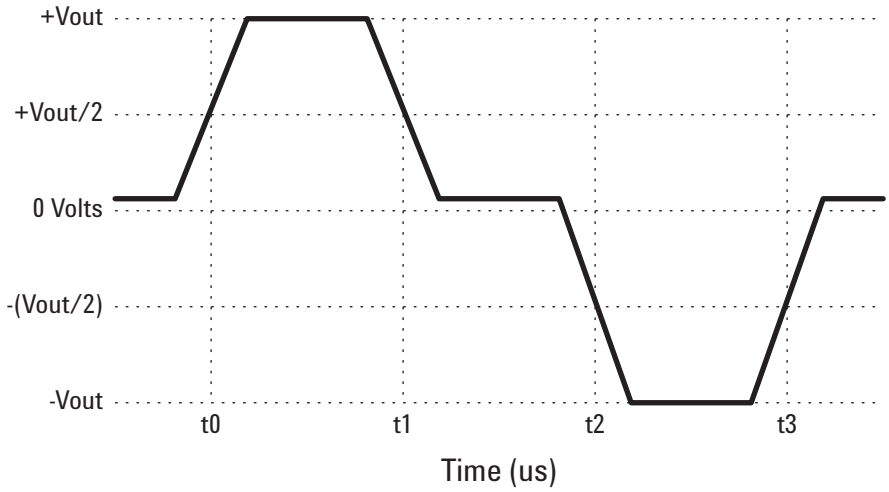


Figure 28 Bottom Threshold

As indicated in Figure 28, the 4 successive 50% crossing times are measured. These are named t0, t1, t2, and t3 respectively. The specification states that the deviations of the 50% crossing times from a best fit grid of 16 ns shall not exceed +/- 250 ps. We validate this specification in terms of the peak-to-peak duty cycle distortion requirement of 500 ps. This is done as follows:

Measure t0, t1, t2, and t3. Then Measure the following time differences between edges, and record the deviation of the actual difference from the expected value:

Table 19 Time Differences Between Edges

Measurement	Expected Value
t1-t0	16 ns
t2-t1	16 ns
t3-t2	16 ns
t2-t0	32 ns
t3-t1	32 ns
t3-t0	48 ns

The largest deviation of these measurements from its expected value is the worst case peak-to-peak duty cycle distortion. For a compliant DUT this worst case DCD must not exceed 500 ps.

Transmitter Return Loss

NOTE This section shows the use of a Vector Network Analyzer (VNA) used for testing Transmitter Return Loss. However, you can use in place of the VNA an exported VNA file in either the Touchstore or CITI file format.

This section describes the 100 Base-TX Transmitter Return Loss test as per ANSI X3.263-1995, Subclause 9.1.5. The test procedures described in this section cover the Transmitter Return Loss measurement required by the specification.

Reference

[1] ANSI X3.263-1995, Subclause 9.1.5

Calibrating the VNA

Before using the VNA, it must be calibrated using the Return Loss Calibration board. See Figure 29 for the connection diagram.

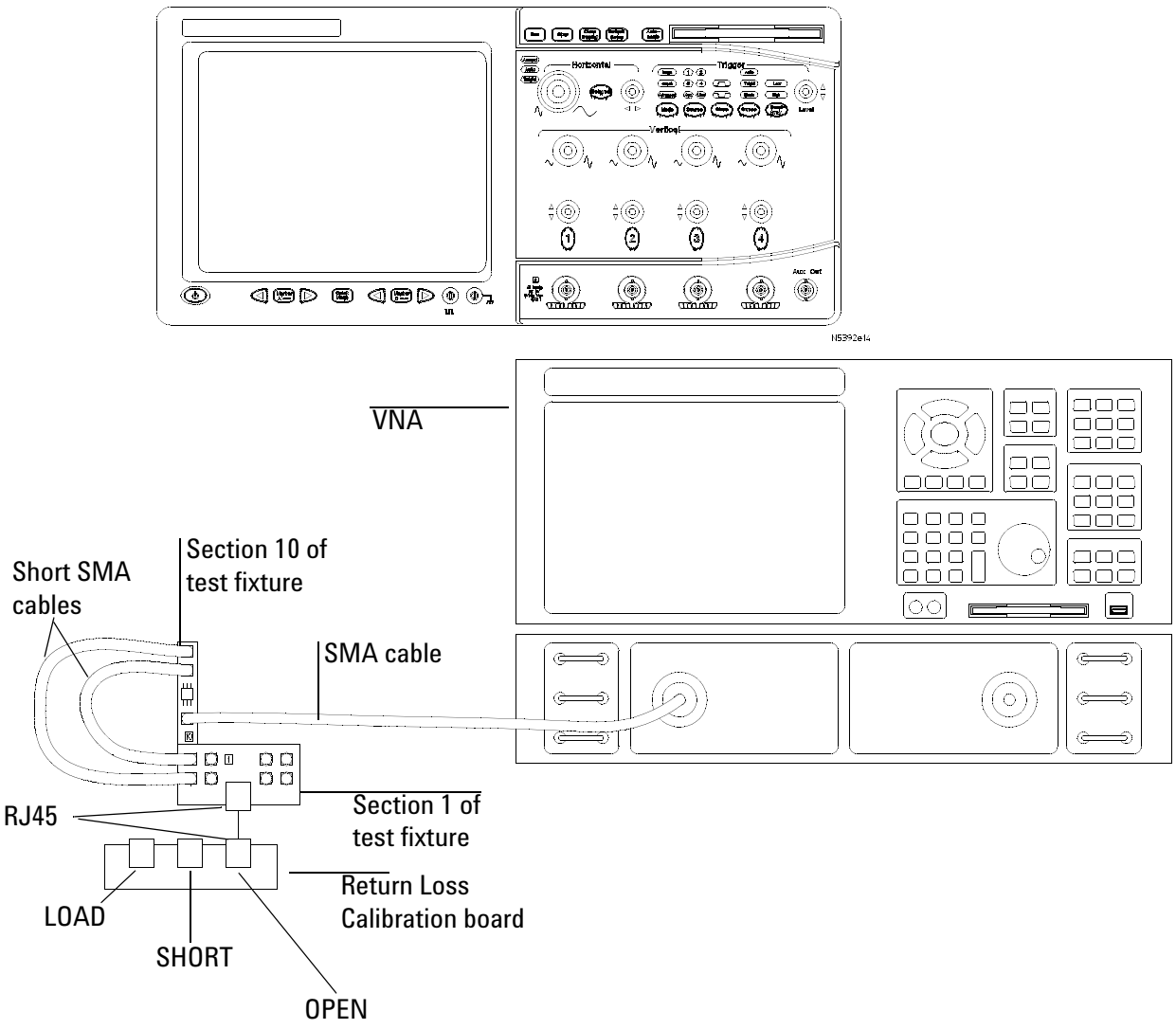


Figure 29 VNA Calibration

1 Connect the Return Loss Calibration board RJ45 connector labeled OPEN to the RJ45 connector on fixture 1 using a short straight-through UTP cable.

2 Connect one end of two short SMA-to-SMA cables to the SMA test points for the pair A you are testing on fixture 1, and the other end to the two SMA (X97 and X98) test points on fixture 10.

3 Connect a VNA input to the SMA (X99) test point on fixture 10.

4 Calibrate the VNA using the instructions in the VNA's User's Guide. The following is a list of setup requirements.

- Set Meas to Ref1 Fwd S11.
- Set Start to 2 MHz.
- Set Stop to 80 MHz.
- Set Format to Log Mag.
- Set Scale Div to 5.
- Set Scale Ref to reference line position 9.

5 Run the calibration for the OPEN, SHORT, and LOAD connections.

Probing Setup for Transmitter Return Loss

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

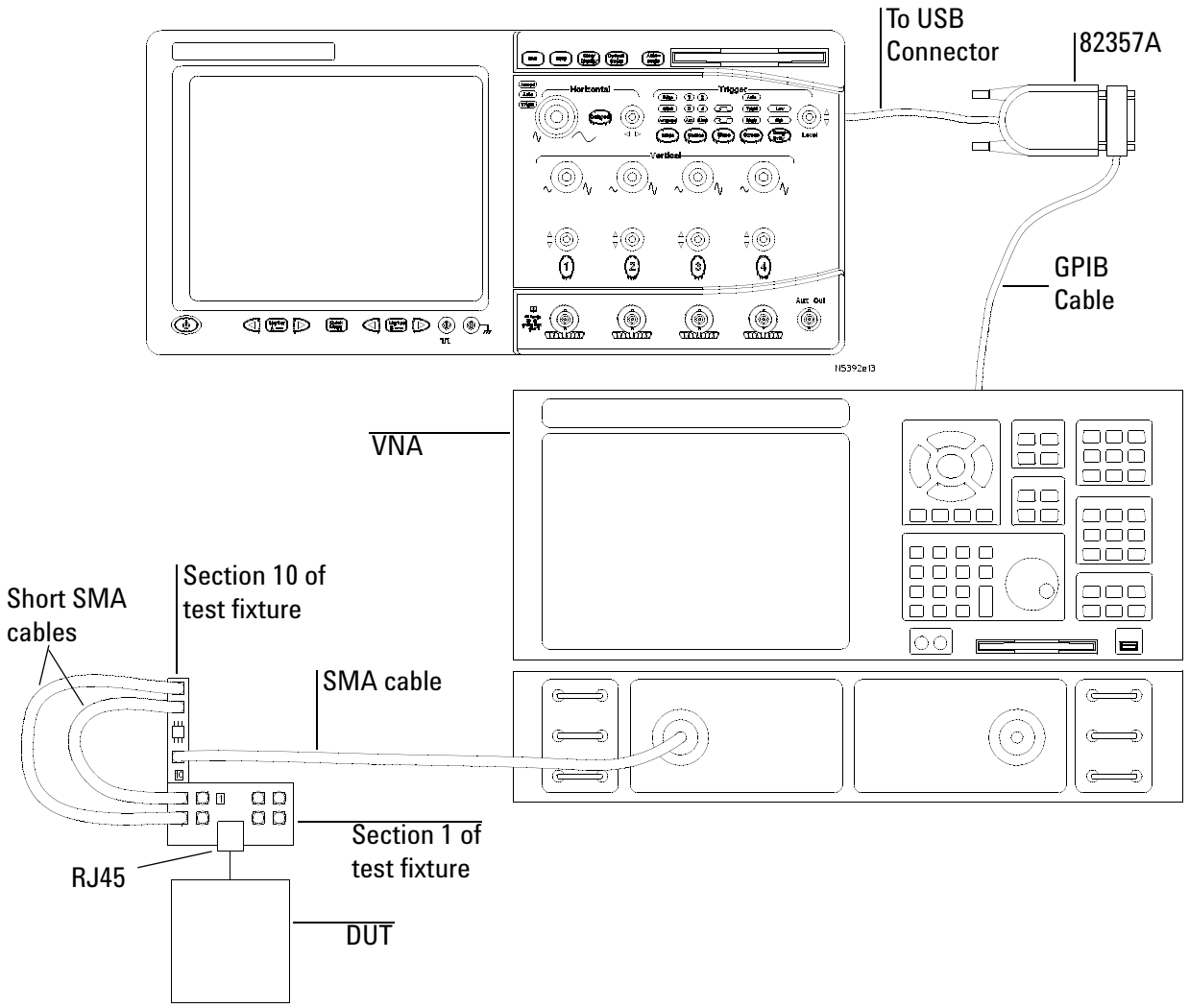


Figure 30 Probing for 100 Base-TX Transmitter Return Loss

1. Connect the DUT to the RJ45 connector on fixture 1 using a short straight-through UTP cable.
2. Connect one end of two short SMA-to-SMA cables to the SMA test points for testing the pair A on fixture 1, and the other end to the two SMA (X97 and X98) test points on fixture 10.
3. Connect a VNA input to the SMA (X99) test point on fixture 10.

4 Connect a GPIB cable to the 82357A GPIB port and to the GPIB port on the VNA.

5 Connect the 82357A USB connector to a USB port on the scope.

Device Configuration

1 Configure the DUT for 100 Base-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded /I/ code-groups.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Compute the return loss as described in the Algorithm Discussion below.

Algorithm Discussion

Reference [1] describes all the receive channel return loss specifications for a 100 Base-T device at the physical medium attachment (PMA). The UTP and STP Active Output Interface shall be implemented such that the following return loss characteristics are satisfied for each of the specified line impedances.

- Greater than 16 dB from 2 MHz to 30 MHz
- Greater than $(16 - 20\log_{10}(f/30\ \text{MHz}))$ dB from 30 MHz to 60 MHz
- Greater than 10 dB from 60 MHz to 80 MHz

The impedance environment for the measurement of the UTP AOI return loss shall be 100 Ω ± 15 Ω; the environment for the STP AOI return loss shall be 150 Ω ± 15 Ω. The impedance environments shall be nominally resistive, with a magnitude of phase angle less than 3° over the specified measurement frequency range.

Receiver Return Loss

NOTE This section shows the use of a Vector Network Analyzer (VNA) used for testing Receiver Return Loss. However, you can use in place of the VNA an exported VNA file in either the Touchstore or CITI file format.

This section describes the 100 Base-TX Receiver Return Loss test as per ANSI X3.263-1995, Subclause 9.2.2. The test procedures described in this section cover the Receiver Return Loss measurement required by the specification.

Reference

[1] ANSI X3.263-1995, Subclause 9.2.2

Calibrating the VNA

Before using the VNA, it must be calibrated using the Return Loss Calibration board. See Figure 31 for the connection diagram.

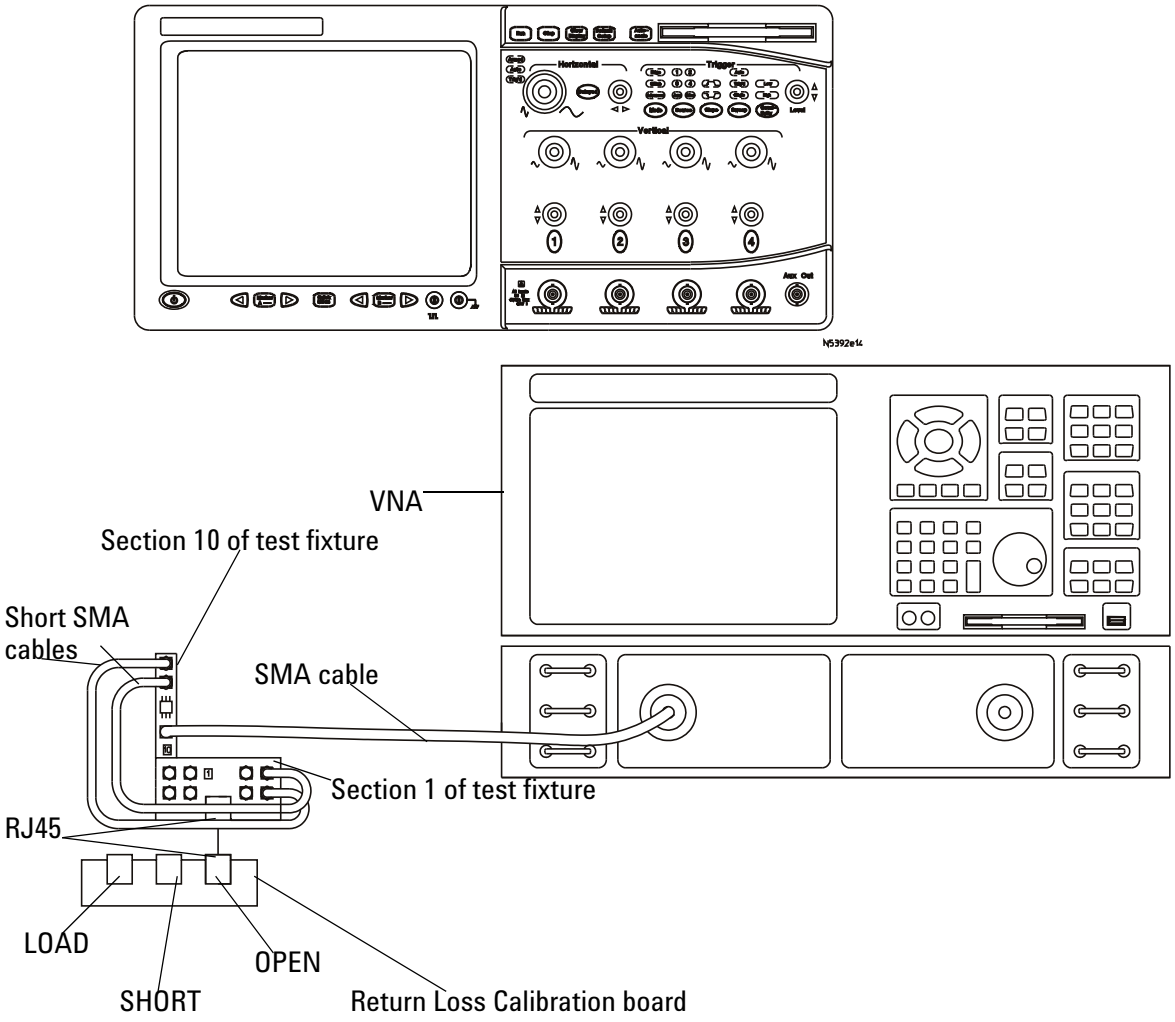


Figure 31 VNA Calibration

1 Connect the Return Loss Calibration board RJ45 connector labeled OPEN to the RJ45 connector on fixture 1 using a short straight-through UTP cable.

2 Connect one end of two short SMA-to-SMA cables to the SMA test points for the pair B you are testing on fixture 1, and the other end to the two SMA (X97 and X98) test points on fixture 10.

3 Connect a VNA input to the SMA (X99) test point on fixture 10.

4 Calibrate the VNA using the instructions in the VNA's User's Guide. The following is a list of setup requirements.

- Set Meas to Ref1 Fwd S11.
- Set Start to 2 MHz.
- Set Stop to 80 MHz.
- Set Format to Log Mag.
- Set Scale Div to 5.
- Set Scale Ref to reference line position 9.

5 Run the calibration for the OPEN, SHORT, and LOAD connections.

Probing Setup for Receiver Return Loss

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

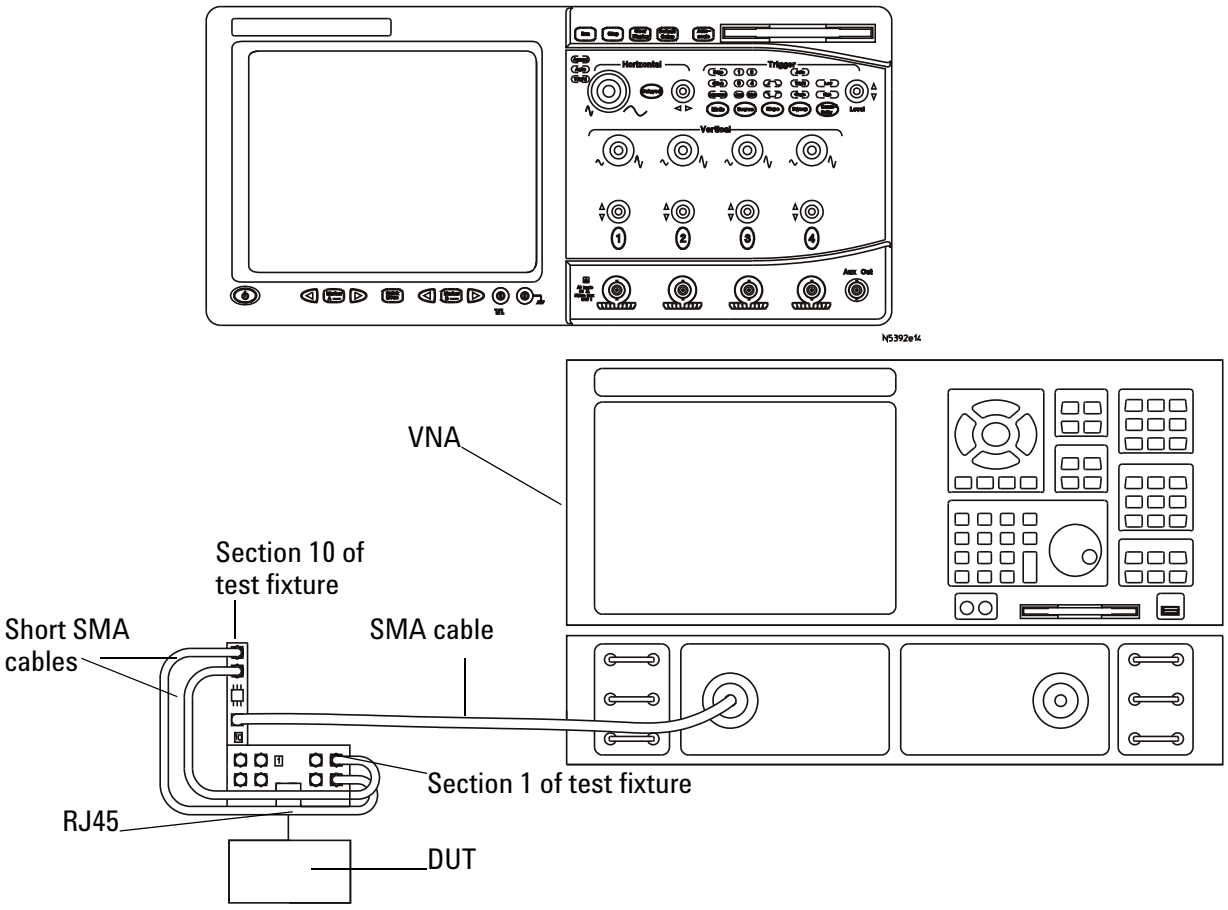


Figure 32 Probing for 100 Base-TX Receiver Return Loss

1 Connect the DUT to the RJ45 connector on fixture 1 using a short straight-through UTP cable.

2 Connect one end of two short SMA-to-SMA cables to the SMA test points for testing the pair B on fixture 1, and the other end to the two SMA (X97 and X98) test points on fixture 10.

3 Connect a VNA input to the SMA (X99) test point on fixture 10.

4 Connect a GPIB cable to the 82357A GPIB port and to the GPIB port on the VNA.

5 Connect the 82357A USB connector to a USB port on the scope.

Device Configuration

1 The DUT for 100 Base-TX operation does not require any particular configuration. Simply turn on the DUT and set the DUT to operate in 100 Base-TX to perform the test.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Compute the return loss as described in the Algorithm Discussion below.

Algorithm Discussion

Reference [1] describes all the receive channel return loss specifications for a 100 Base-T device at the physical medium attachment (PMA). The differential input impedance shall be such that the return loss is shown below. The requirement is specified for any reflection due to differential signals incident upon RX+/- from a twisted pair having any impedance within the range specified in ANSI X3.263-1995 Subclause 11.1.1. The return loss shall be maintained when the receiver circuit is powered.

- Greater than 16 dB from 2 MHz to 30 MHz
- Greater than $(16 - 20\log_{10}(f/30\ \text{MHz}))$ dB from 30 MHz to 60 MHz
- Greater than 10 dB from 60 MHz to 80 MHz

6
10 Base-T Tests

Test Loads

Some of the 10 Base-T tests require the use of special loads. Three different loads are defined. Load 1 and Load 2 are defined in Figure 14-11 of IEEE 802.3-2008, sub clause 14.3.1.2.2. Load 3 (100 ohms) is defined as a 100 ohm resistive load.

Measurements with TPM, Template Tests

Sub clause 14.3.1.2 of IEEE 802.3-2008 defines the transmitter specifications for a 10 Base-T Medium Access Unit (MAU) the MAU-to-MDI interface. Some of these tests require the use of an equivalent circuit that models the distortion of a simplex link segment. This is called the Twisted Pair Model (or TPM). The specifications for the TPM are listed in figure 14-7 of IEEE 802.3-2008, sub clause 14.3.1.2. These tests use section 7 of the Ethernet Electrical Compliance Test Fixture ("10BT with TP Model"). To simplify test setup, tests requiring the TPM (section 7 of the test fixture) are organized in one section.

Probing for 10 Base-T Tests With the TPM and Link Partner

These probing instructions apply to tests that use the twisted pair model (TPM) and a link partner. Note that some tests (link test pulse template) do not require the use of a link partner. Instructions for those tests are provided in the section for the test.

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

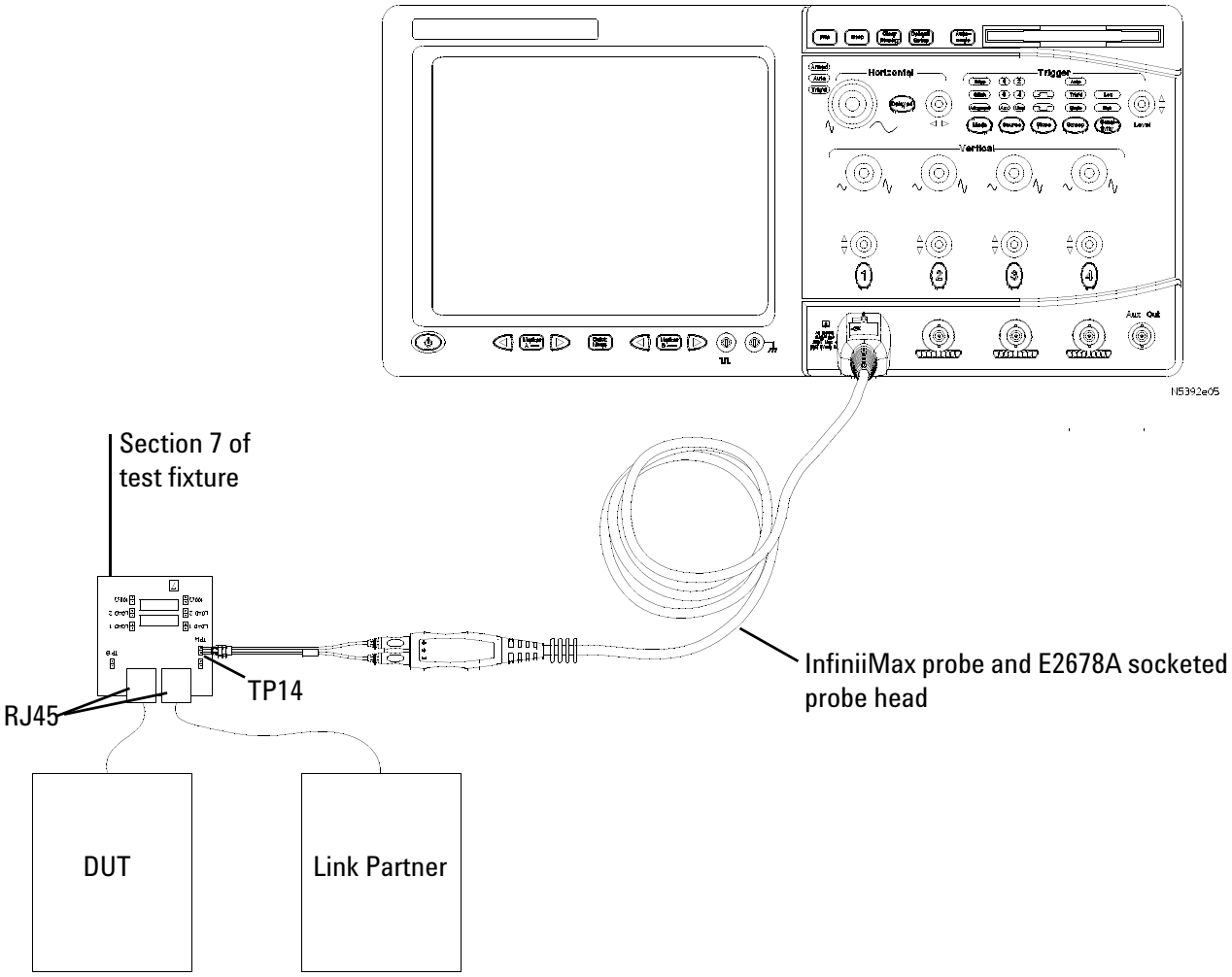


Figure 33 Probing for 10 Base-T Tests With the TPM and Link Partner

1. Connect the DUT to the RJ45 connector on fixture 7 marked DUT (J9) using a short UTP cable.
2. Connect a 10 Base-T link partner to the RJ45 connector on fixture 7 marked Link Port (J8) using a short UTP cable.
3. Connect an InfiniiMax differential probe with E2678A differential socketed probe head to TP14 and to the configured “DUT Data” channel on the oscilloscope. This setting is shown in the Configure tab.
4. Using two jumpers, short the appropriate load on fixture 7. This setting is shown in the Configure tab and the loads are labeled on the fixture 7.

Link Test Pulse, with TPM

This test ensures that the link test pulse falls within the shaded area of figure 14-10 of IEEE 802.3-2008, sub clause 14.3.1.2.1. This measurement is to be made with the 3 different loads as defined in “Test Loads" on page 130. This test measures the signal across the appropriate load, with the load connected through the twisted pair model (TPM) as defined in figures 14-7 and 14-8 of IEEE 802.3-2008, sub clause 14.3.1.2.

References

[1] IEEE 802.3-2008, Sub clause 14.3.1.2.1.

[2] IEEE 802.3-2008, Sub clause 14.3.1.2.2.

Probing Setup

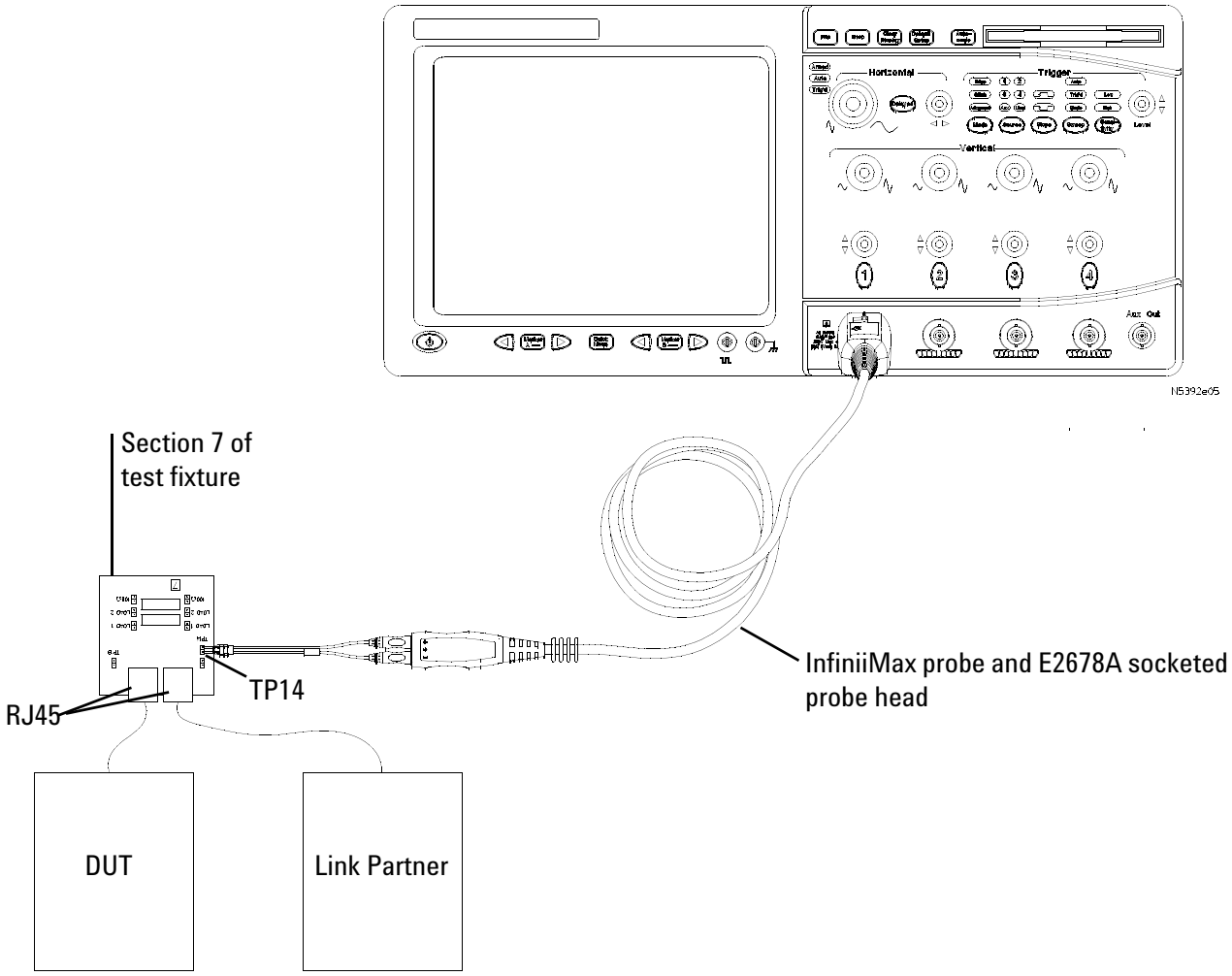


Figure 34 Probing for 10 Base-T Tests With the TPM and Link Partner

1 Connect the DUT to the RJ45 connector on fixture 7 marked DUT (J9) using a short UTP cable.

2 Connect a 10 Base-T link partner to the RJ45 connector on fixture 7 marked Link Port (J8) using a short UTP cable.

3 Connect an InfiniiMax differential probe with E2678A differential socketed probe head to TP14 with the plus (+) side of the probe head connected to the plus (+) side of TP14. Connect the other end of the probe to the oscilloscope channel selected for “DUT Data” as shown in the Connect tab.

4 Using two jumpers, short the appropriate load on fixture 7. This setting is shown in the Configure tab and the loads are labeled on the fixture 7.

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

Configuring the Device Under Test (DUT)

1 Reset the DUT if necessary.

2 Ensure that the DUT is transmitting the proper Link Test Pulse as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel.
- Configure the oscilloscope to capture the link test pulse.
- Load the mask for the start of the link test pulse.
- Capture a (user configurable) number of pulses (with user defined amount of averaging), testing each pulse against start of the mask.
- Record the number of mask failures for the start of the link test pulse.
- Load the mask for the end of the link test pulse.
- Capture a (user configurable) number of pulses (with user defined amount of averaging), testing each pulse against the end of the mask.
- Record the number of mask failures for the end of the link test pulse.
- Compute the total number of failures (start + end).

NOTE If you have selected "ALL" as the "10 Base-T LTP/TP_IDL Loads" (under the Configure tab), the 3 required loads will be tested in sequence. You will be prompted to short each load (with jumpers) in turn, and this measurement will be repeated with each load. If you want to debug a particular load, select "Debug Mode" in the Configure tab, and select the individual load you wish to test. Note that for full compliance testing, you should test all 3 loads. At the result screen, 3 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Load 1 result, Trial 2 contains Load 2 result and so on.

Algorithm Discussion

Reference [1] defines the link-test pulse template specifications a 10 Base-T Medium Access Unit (MAU) at the MAU-to-MDI interface. This test requires the use of the twisted pair model (TPM) as defined in figure 14-7 of IEEE 802.3-2008, sub clause 14.3.1.2.

This test ensures that the link test pulse falls within the shaded area of figure 14-12 of Reference [1]. This measurement is to be made with the 3 different loads as defined in "Test Loads" on page 130. This test measures the signal with across the appropriate load, with the load connected through the twisted pair model (TPM).

Because the mask is defined over a large number of bits, measurement performance is improved by testing the signal against the mask in two sections. We test the start of the link-test pulse separately from the end of the link test pulse.

A user configurable number of waveforms are tested against the mask. Note that if the MAU implements the auto negotiation algorithm defined in IEEE 802.3-2008, clause 28, the FLP (fast link pulse) burst sequence will consist of multiple link test pulses. All link test pulses in the FLP burst sequence should pass the template requirements. Agilent recommends testing a large number of pulses to ensure that all link-test pulses in the FLP burst sequence have been observed. The default number of waveforms tested is 100 for this test. The default number of averages is 512.

A user configurable amount of averaging is also utilized to reduce vertical noise errors. The algorithm proceeds as described in the above section "Performing the Test".

NOTE The template requirements for this test are specified in such a way that testing with a digital oscilloscope is often impractical. Specifically, the large vertical and horizontal range of the masks will often result in failures when applying automated template test techniques. Specifically, you should exercise your own judgement when failures are marginal to determine if the signal shape is satisfactory.

TP_IDL Template, with TPM

This test ensures that the TP_IDL signal falls within the shaded area of figure 14-10 of IEEE 802.3-2008, subclause 14.3.1.2.1. This measurement is to be made with the 3 different loads as defined in “Test Loads" on page 130. This test measures the signal across the appropriate load, with the load connected through the twisted pair model (TPM) as defined in figures 14-7 and 14-8 if IEEE 802.3-2008, subclause 14.3.1.2.

References

[1] IEEE 802.3-2008, Subclause 14.3.1.2.1.

Probing Setup

NOTE Before starting a test, you can view these connection instructions under the application’s Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

Refer to “Probing for 10 Base-T Tests With the TPM and Link Partner" on page 131.

1 Ensure that you short the appropriate load, as indicated in the connectivity instructions in the user interface.

2 Ensure the correct probe polarity.

Device Configuration

1 Reset the DUT if necessary

2 Configure the DUT to output 10 Base-T random data (see “Configuring a 10 Base-T Device to Output Random Data" on page 166).

3 Ensure that the oscilloscope is capturing proper signal (TP_IDL) as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Determine the widths of the different TP_IDL pulses. (For a given device, there are two different TP_IDL pulse widths, depending on the value of the last bit in the packet.)
- For each of the different TP_IDL pulse widths:
  - Verify that the correct test signal is present on the configured "DUT Data" channel.
  - Configure the oscilloscope to capture this width TP_IDL signal using a user-configurable amount of averaging. This reduces measurement noise and increases measurement accuracy.

NOTE Averaging here is only valid because we are isolating the different pulse widths before averaging.

- Load the mask for the start of the TP_IDL signal.
- Capture a (user configurable) number of pulses (with user defined amount of averaging), testing each pulse against start of the mask.
- Record the number of mask failures for the start of the TP_IDL signal.
- Load the mask for the end of the TP_IDL signal.
- Capture a (user configurable) number of pulses testing each pulse against the end of the mask.
- Record the number of mask failures for the end of the TP_IDL signal.
- Compute the total number of failures (start + end).

NOTE If you have selected "ALL" as the "10 Base-T LTP/TP_IDL Loads" (under the Configure tab), the 3 required loads will be tested in sequence. You will be prompted to short each load (with jumpers) in turn, and this measurement will be repeated with each load. If you want to debug a particular load, select "Debug Mode" in the Configure tab, and select the individual load you wish to test. Note that for full compliance testing, you should test all 3 loads. At the result screen, 3 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Load 1 result, Trial 2 contains Load 2 result and so on.

Algorithm Discussion

Reference [1] defines the TP_IDL template specifications a 10 Base-T Medium Access Unit (MAU) at the MAU-to-MDI interface. This test requires the use of the twisted pair model (TPM) as defined in figure 14-7 of IEEE 802.3-2008, subclause 14.3.1.2.

This test ensures that the TP_IDL signal falls within the shaded area of figure 14-10 of Reference [1]. This measurement is to be made with the 3 different loads as defined in "Test Loads" on page 130. This test measures the signal across the appropriate load, with the load connected through the twisted pair model (TPM).

Because the mask is defined over a large number of bits, measurement performance is improved by testing the signal against the mask in two sections. We test the start of the TP_IDL separately from the end of the TP_IDL.

The TP_IDL signal indicates the end of a transmitted data sequence. As stated in Reference [1], if the last bit transmitted was a CD1, the last transition will be at the bit cell center of the CD1. If the last bit transmitted was a CD0, the PLS will generate an addition transition at the bit cell boundary following the CD0. After the zero crossing of the last transition, the differential voltage shall remain within the shaded area of Figure 14-10 of Reference [1].

NOTE Because there are two distinct TP_IDL pulses of different widths (depending on the last bit transmitted), signal averaging would produce an invalid edge between the two real TP_IDL pulses. Averaging these two pulses would produce a signal that is not representative of either of the real TP_IDL pulses, so averaging is generally not a valid technique. The N5392A Ethernet compliance test application overcomes this problem by isolating the different TP_IDL pulses and averaging together only pulses of that width. This increases the amount of waveform captures required to make a pass/fail determination, but it greatly improves the measurement accuracy.

A user configurable number of waveforms are tested against the mask. The default number of waveforms tested is 100 for this test. The default number of averages is 512. The algorithm proceeds as described in the above section "Performing the Test".

NOTE The template requirements for this test are specified in such a way that testing with a digital oscilloscope is often impractical. Specifically, the large vertical and horizontal range of the masks will often result in failures when applying automated template test techniques. Specifically, you should exercise your own judgement when failures are marginal to determine if the signal shape is satisfactory.

NOTE Because the oscilloscope uses special triggering capabilities to qualify both variants of TP_IDL, this test can run slowly. One way to significantly speed up this test is to send very short packets so that the TP_IDL signal occurs frequently.

MAU Template

This test ensures that the signal Vo, defined at the output of the twisted pair model (TPM), as defined in figure 14-8 of IEEE 802.3-2008, subclause 14.3.1.2.1, falls within the template defined in Figure 14-9 and Table 14-1 (integrated and external MAU) of IEEE 802.3-2008, subclause 14.3.1.2.1 for all data sequences. This measurement is to be made only with the TPM, and only with the 100 ohm load. This test measures the signal across the appropriate load, with the load connected through the twisted pair model (TPM) as defined in figures 14-7 and 14-8 if IEEE 802.3-2008, subclause 14.3.1.2. This test is run with the DUT configured to output 10 Base-T Random Data.

References

[1] IEEE 802.3-2008, Subclause 14.3.1.2.1.

Probing Setup

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

Refer to "Probing for 10 Base-T Tests With the TPM and Link Partner" on page 131.

1. Ensure that you short the appropriate load, as indicated in the connectivity instructions in the user interface.
2. Ensure the correct probe polarity.

Device Configuration

1. Reset the DUT if necessary.
2. Configure the DUT to output 10 Base-T random data (see "Configuring a 10 Base-T Device to Output Random Data" on page 166).
3. Ensure that the oscilloscope is capturing proper signal (10 Base-T Random Data) as indicated in the connection instructions provided in the user interface.

Performing the Test

1. Ensure this test is checked to run in the "Select Tests" tab.
2. Press the "Run Tests" button in the task flow to start testing
3. If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have

completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel.
- Configure the oscilloscope to capture the 10 Base-T Random Data signal, triggering on the rising edge of the data.
- Load the appropriate mask for the rising data edge:
  - Two masks are supported. Depending on the MAU Type (Integrated or External) MAU, as defined in Table 14-1 of Reference [1]. You can select the 10 Base-T MAU type under the Configure tab.
- Scale the mask for the best fit. The template voltage may be scaled by a factor of 0.9 to 1.1, but any scaling below 0.9 or above 1.1 is not allowed.
- Capture a (user configurable) number of waveforms, testing each waveform against the mask.
- Record the number of mask failures for the rising data edge mask.
- Configure the oscilloscope to capture the 10 Base-T Random Data signal, triggering on the rising edge of the data.
- Invert the rising edge data mask about the time axis
- Scale the mask for the best fit. The template voltage may be scaled by a factor of 0.9 to 1.1, but any scaling below 0.9 or above 1.1 is not allowed.
- Capture a (user configurable) number of waveforms, testing each waveform against the mask.
- Record the number of mask failures for the falling data edge mask.
- Compute the total number of failures (rising + falling).

Algorithm Discussion

Reference [1] defines the internal and external MAU template specifications a 10 Base-T Medium Access Unit (MAU) at the MAU-to-MDI interface. This test requires the use of the twisted pair model (TPM) as defined in figure 14-7 of IEEE 802.3-2008, subclause 14.3.1.2.

This test ensures that the signal Vo, defined at the output of the twisted pair model (TPM), as defined in figure 14-18 of Reference [1], falls within the template defined in Figure 14-9 and Table 14-1 (integrated and external MAU) of Reference [1] for all data sequences. During the test the TPM is terminated in 100 ohms and driven by a transmitter with a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

Mask normalization is performed by scaling the mask relative to the signal. Scaling below 0.9 or above 1.1 is not allowed. Two types of MAU masks are supported: integrated and external. The user should select the MAU type in the Configure tab under 10 Base-T MAU Type. The appropriate mask is loaded for the MAU Type selected.

The test is run for data sequences starting with rising and falling edges. These two tests are conducted separately with the mask inverted about the time axis for the falling edge test. The total number of failures should be zero for a compliant device.

A user configurable number of waveforms are tested against the mask. The default number of waveforms is 100 for this test. You may wish to increase this number for more complete validation. The algorithm proceeds as described in the above section "Performing the Test".

NOTE

The template requirements for this test are specified in such a way that testing with a digital oscilloscope is often impractical. Specifically, the large vertical and horizontal range of the masks will often result in failures when applying automated template test techniques. Specifically, you should exercise your own judgement when failures are marginal to determine if the signal shape is satisfactory.

Measurements with TPM, Parametric Tests

Subclause 14.3.1.2 of IEEE 802.3-2008 defines the transmitter specifications a 10 Base-T Medium Access Unit (MAU) the MAU-to-MDI interface. Some of these tests require the use of an equivalent circuit that models the distortion of a simplex link segment. This is called the Twisted Pair Model (or TPM). The specifications for the TPM are listed in figure 14-7 of IEEE 802.3-2008, subclause 14.3.1.2. These tests utilize section 7 of the Ethernet Electrical Compliance Test Fixture ("10BT with TP Model"). To simplify test setup, tests requiring the TPM (section 7 of the test fixture) are organized in one section.

Jitter with TPM

This test ensures that the transmitter output jitter measured at the output of the twisted pair model (TPM), as defined in figure 14-18 of IEEE 802.3-2008, subclause 14.3.1.2.1, is within conformance limits. Jitter is measured with and without the TPM. This test measures jitter with the TPM. The jitter measurement is made with the TPM terminated in the 100 ohm resistive load. This test is run with the DUT configured to output 10 Base-T Random Data.

References

[1] IEEE 802.3-2008, Subclause 14.3.1.2.3.

[2] IEEE 802.3-2008, Annex B.4.3.3.

[3] IEEE 802.3-2008, Annex B.4.1 "System Jitter budget".

Probing Setup

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

Refer to "Probing for 10 Base-T Tests With the TPM and Link Partner" on page 131.

1 Ensure that you short the appropriate load, as indicated in the connectivity instructions in the user interface.

2 Ensure the correct probe polarity.

Device Configuration

1 Reset the DUT if necessary

2 Configure the DUT to output 10 Base-T random data (see “Configuring a 10 Base-T Device to Output Random Data" on page 166).

3 Ensure that the oscilloscope is capturing proper signal (10 Base-T Random Data) as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel.
- Configure the oscilloscope to capture the 10 Base-T Random Data signal.
- Attempt, if Jitter Trigger Method is configured as “Automatic”, to determine the packet size and establish a stable trigger on a rising edge in the middle of the packet. If Jitter Trigger Method is configured as “Manual”, it will prompt you to configure the trigger system appropriately.
- Render the zero crossings at 8.0 BT or 8.5 BT, depending on the user selection for "10 Base-T Jitter Measurement" in the Configure tab.
- Continue to acquire and displaying waveforms until a user configurable number of jitter waveforms have been observed.
- Place a waveform histogram at the 0 V level, and measure the minimum and maximum deviation from the ideal edge location (8.0 BT or 8.5 BT).
- Ensure that the worst deviation is within conformance limits as listed in the Algorithm Discussion.

NOTE If you have selected "ALL" as the "10 Base-T Jitter Measurement" (under the Configure tab), this test will be run at 8.0 BT and 8.5 BT. If you want to debug the 8.0 BT or 8.5 BT separately, select "Debug Mode" in the Configure tab, and select the individual test you wish to run. Note that for full compliance testing, you should test at both 8.0 BT and 8.5 BT as described in Reference[2]. At the result screen, 2 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains 8.0 BT result, Trial 2 contains 8.5 BT result and so on.

Algorithm Discussion

Reference [1] defines the integrated and external jitter specifications a 10 Base-T Medium Access Unit (MAU) at the MAU-to-MDI interface. This test requires the use of the twisted pair model (TPM) as defined in figure 14-7 of IEEE 802.3-2008, subclause 14.3.1.2.

Testing with the TPM (cable) validates the maximum-length twisted-pair link as defined in annex B.4.1 System jitter budget. During the test the TPM is terminated in 100 ohms and driven by a transmitter with a Manchester-encoded pseudorandom sequence with a minimum repetition period of 511 bits.

In accordance with Annex B.4.3.3, An external MAU with a jitterless source driving DO is compliant when all zero crossings fall within the time ranges listed in Table 20. Two constraints are required: 8.0 bit time crossings and 8.5 bit time crossings. According to annex B.4.3.3 Note for 14.3.1.2.3 on output timing jitter, these two constraints completely determine compliance or noncompliance.

Table 20 Jitter Measurements* with TPM (cable)

MAU Type	Measurement	Limits
External	8.0 BT	8.0 BT +/- 7.0 ns
External	8.5 BT	8.5 BT +/- 7.0 ns
Internal	8.0 BT	8.0 BT +/- 11.0 ns
Internal	8.5 BT	8.5 BT +/- 11.0 ns

*The Jitter constraints are as per Reference[3].

A user configurable number of waveforms are acquired/analyzed for each measurement. The default number of waveforms is 10,000 for this test. You may wish to increase this number for more complete validation, or decrease it to speed up test time. The algorithm proceeds as described in the above section "Performing the Test".

Measurements without TPM, Template Tests

Subclause 14.3.1.2 of IEEE 802.3-2008 defines the transmitter specifications a 10 Base-T Medium Access Unit (MAU) the MAU-to-MDI interface. Some of these tests require the use of an equivalent circuit that models the distortion of a simplex link segment. This is called the Twisted Pair Model (or TPM). There are also a number of tests that do not utilize the twisted pair model. To simplify test setup, tests performed without the TPM (section 6 of the test fixture, marked “10BT without TP Model”) are organized in one section.

Probing for 10 Base-T Tests Without the TPM, With Link Partner

These probing instructions apply to tests that do not use the twisted pair model (TPM), and typically require a link partner. Note that some tests (link test pulse template) do not require the use of a link partner. Instructions for those tests are provided in the section for the test.

NOTE Before starting a test, you can view these connection instructions under the application’s Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

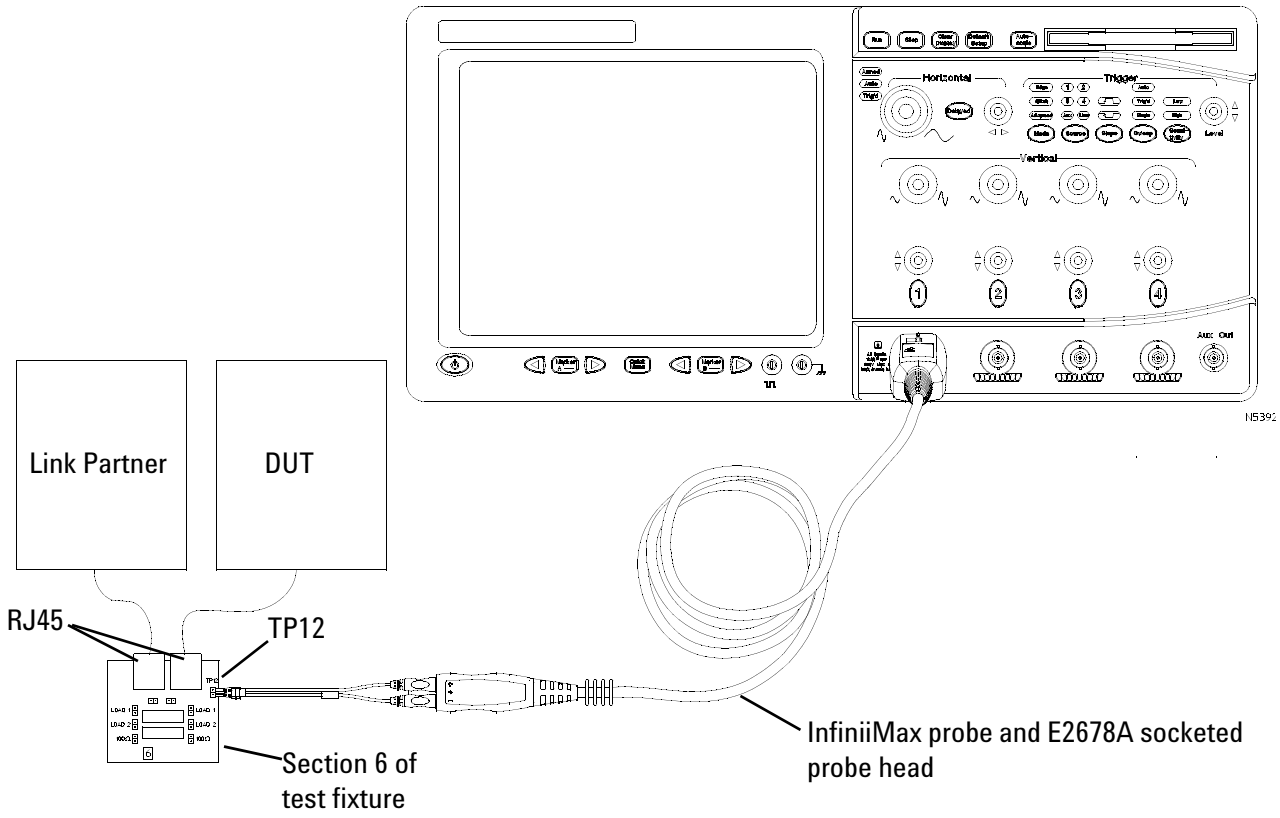


Figure 35 Probing for 10 Base-T Tests Without the TPM, With Link Partner

1 Connect the DUT to the RJ45 connector on fixture 6 marked DUT (J6) using a short UTP cable.

2 Connect a 10 Base-T link partner to the RJ45 connector on fixture 6 marked LP (J7) using a short UTP cable.

3 Connect an InfiniiMax differential probe with E2678A differential socketed probe head to TP12 and to the configured “DUT Data” channel on the oscilloscope.

4 Using two jumpers, short the appropriate load on fixture 6. The loads are labeled on the fixture.

NOTE Do not place shorting jumpers across JP40 or JP39 as this can case the test to fail.

Link Test Pulse, without TPM

This test ensures that the link test pulse falls within the shaded area of figure 14-12 of IEEE 802.3-2008, subclause 14.3.1.2.1. This measurement is to be made with the 3 different loads as defined in “Test Loads" on page 130. This test measures the signal across the appropriate load, with the load connected directly to the TD circuit as defined in figure 14-8 of IEEE 802.3-2008, subclause 14.3.1.2.

References

[1] IEEE 802.3-2008, Subclause 14.3.1.2.1.

[2] IEEE 802.3-2008, Subclause 14.3.1.2.2.

Probing Setup

NOTE Before starting a test, you can view these connection instructions under the application’s Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

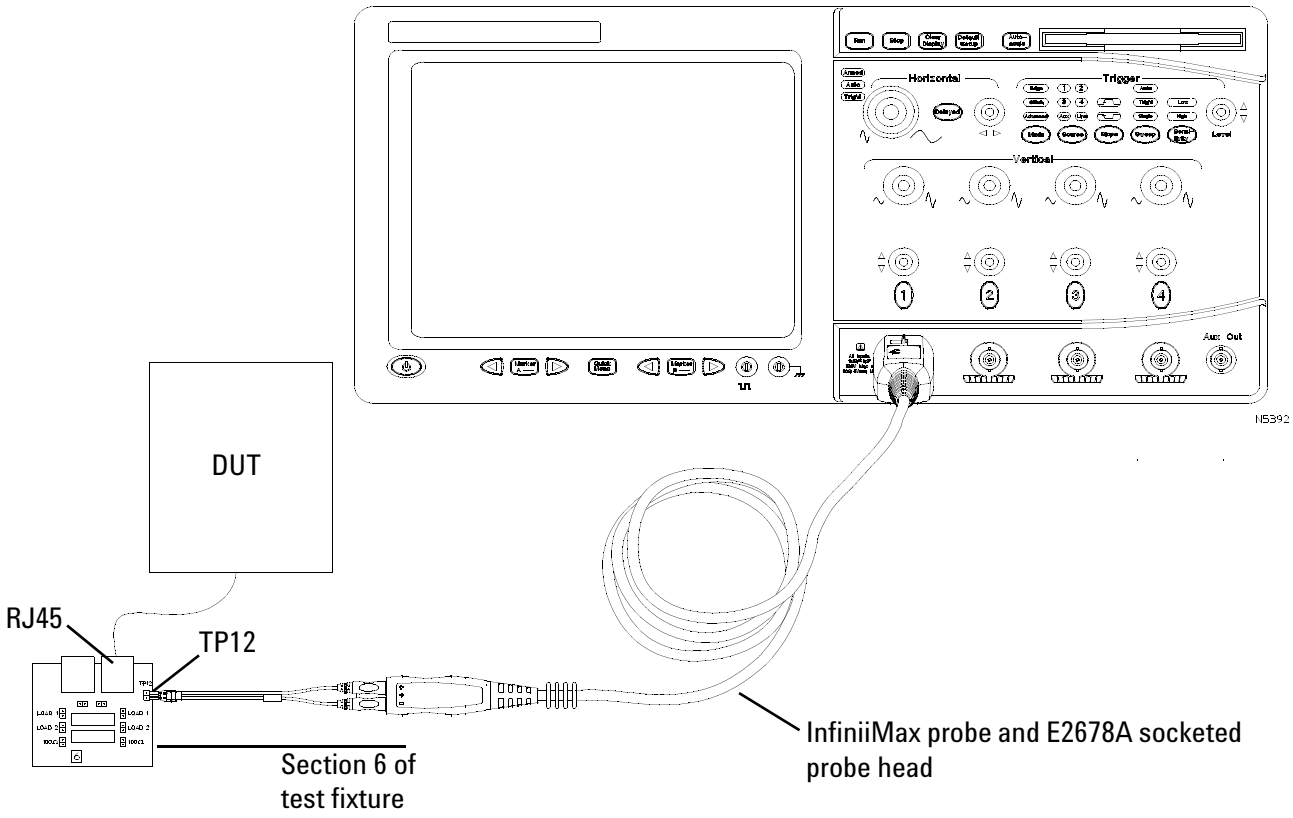


Figure 36 Probing for 10 Base-T Link Test Pulse, Without TPM

1 Connect the DUT to the RJ45 connector on fixture 6 marked DUT (J6) using a short UTP cable.

2 Connect an InfiniiMax differential probe with E2678A differential socketed probe head to TP12 and to the configured “DUT Data” channel on the oscilloscope.

3 Using two jumpers, short the appropriate load on fixture 6.

NOTE Do not place shorting jumpers across JP40 or JP39 as this can case the test to fail.

Device Configuration

1 Reset the DUT if necessary.

2 Ensure that the DUT is transmitting the proper signal (link test pulse) as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel.
- Configure the oscilloscope to capture the link test pulse.
- Load the mask for the start of the link test pulse.
- Capture a (user configurable) number of pulses (with user defined amount of averaging), testing each pulse against start of the mask.
- Record the number of mask failures for the start of the link test pulse.
- Load the mask for the end of the link test pulse.
- Capture a (user configurable) number of pulses (with user defined amount of averaging), testing each pulse against the end of the mask.
- Record the number of mask failures for the end of the link test pulse.
- Compute the total number of failures (start + end).

NOTE If you have selected "ALL" as the "10 Base-T LTP/TP_IDL Loads" (under the Configure tab), the 3 required loads will be tested in sequence. You will be prompted to short each load (with jumpers) in turn, and this measurement will be repeated with each load. If you want to debug a particular load, select "Debug Mode" in the Configure tab, and select the individual load you wish to test. Note that for full compliance testing, you should test all 3 loads. At the result screen, 3 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Load 1 result, Trial 2 contains Load 2 result and so on.

Algorithm Discussion

Reference [1] defines the link-test pulse template specifications a 10 Base-T Medium Access Unit (MAU) at the MAU-to-MDI interface. This test is performed without the twisted pair model (TPM). This test ensures that the link test pulse falls within the shaded area of figure 14-12 of Reference [1]. This measurement is to be made with the 3 different loads

as defined in “Test Loads" on page 130. This test measures the signal with across the appropriate load, with the load connected directly to the TD circuit as defined in Figure 14-8 of Reference [1].

Because the mask is defined over a large number of bits, measurement performance is improved by testing the signal against the mask in two sections. We test the start of the link-test pulse separately from the end of the link test pulse.

A user configurable number of waveforms are tested against the mask. Note that if the MAU implements the auto negotiation algorithm defined in IEEE 802.3-2008, clause 28, the FLP (fast link pulse) burst sequence will consist of multiple link test pulses. All link test pulses in the FLP burst sequence should pass the template requirements. Agilent recommends testing a large number of pulses to ensure that all link-test pulses in the FLP burst sequence have been observed. The default number of waveforms tested is 100 for this test. The default number of averages is 512.

A user configurable amount of averaging is also utilized to reduce vertical noise errors. The algorithm proceeds as described in the above section "Performing the Test".

NOTE The template requirements for this test are specified in such a way that testing with a digital oscilloscope is often impractical. Specifically, the large vertical and horizontal range of the masks will often result in failures when applying automated template test techniques. Specifically, you should exercise your own judgement when failures are marginal to determine if the signal shape is satisfactory.

TP_IDL Template, without TPM

This test ensures that the TP_IDL signal falls within the shaded area of figure 14-10 of IEEE 802.3-2008, subclause 14.3.1.2.1. This measurement is to be made with the 3 different loads as defined in “Test Loads" on page 130. This test measures the signal across the appropriate load, with the load connected directly to the TD circuit as defined in figure 14-8 of IEEE 802.3-2008, subclause 14.3.1.2.1.

References

[1] IEEE 802.3-2008, Subclause 14.3.1.2.1.

Probing Setup

NOTE Before starting a test, you can view these connection instructions under the application’s Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

Refer to “Probing for 10 Base-T Tests Without the TPM, With Link Partner" on page 146.

1 Ensure that you short the appropriate load, as indicated in the connectivity instructions in the user interface.

2 Ensure the correct probe polarity.

Device Configuration

1 Reset the DUT if necessary

2 Configure the DUT to output 10 Base-T random data (see “Configuring a 10 Base-T Device to Output Random Data" on page 166).

3 Ensure that the oscilloscope is capturing proper signal (TP_IDL) as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Determine the widths of the different TP_IDL pulses. (For a given device, there are two different TP_IDL pulse widths, depending on the value of the last bit in the packet.)
- For each of the different TP_IDL pulse widths:
  - Verify that the correct test signal is present on the configured "DUT Data" channel.
  - Configure the oscilloscope to capture this width TP_IDL signal using a user-configurable amount of averaging. This reduces measurement noise and increases measurement accuracy.

NOTE Averaging here is only valid because we are isolating the different pulse widths before averaging.

  - Load the mask for the start of the TP_IDL signal.
  - Capture a (user configurable) number of pulses (with user defined amount of averaging), testing each pulse against start of the mask.
  - Record the number of mask failures for the start of the TP_IDL signal.

- Load the mask for the end of the TP_IDL signal.
- Capture a (user configurable) number of pulses testing each pulse against the end of the mask.
- Record the number of mask failures for the end of the TP_IDL signal.
- Compute the total number of failures (start + end).

NOTE If you have selected "ALL" as the "10 Base-T LTP/TP_IDL Loads" (under the Configure tab), the 3 required loads will be tested in sequence. You will be prompted to short each load (with jumpers) in turn, and this measurement will be repeated with each load. If you want to debug a particular load, select "Debug Mode" in the Configure tab, and select the individual load you wish to test. Note that for full compliance testing, you should test all 3 loads. At the result screen, 3 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains Load 1 result, Trial 2 contains Load 2 result and so on.

Algorithm Discussion

Reference [1] defines the TP_IDL template specifications a 10 Base-T Medium Access Unit (MAU) at the MAU-to-MDI interface. This test is performed without the twisted pair model (TPM).

This test ensures that the TP_IDL signal falls within the shaded area of figure 14-10 of Reference [1]. This measurement is to be made with the 3 different loads as defined in "Test Loads" on page 130. This test measures the signal across the appropriate load, with the load connected directly to the TD circuit as defined in figure 14-8 of Reference [1].

Because the mask is defined over a large number of bits, measurement performance is improved by testing the signal against the mask in two sections. We test the start of the TP_IDL separately from the end of the TP_IDL.

The TP_IDL signal indicates the end of a transmitted data sequence. As stated in Reference [1], if the last bit transmitted was a CD1, the last transition will be at the bit cell center of the CD1. If the last bit transmitted was a CD0, the PLS will generate an addition transition at the bit cell boundary following the CD0. After the zero crossing of the last transition, the differential voltage shall remain within the shaded area of Figure 14-10 of Reference [1].

NOTE Because there are two distinct TP_IDL pulses of different widths (depending on the last bit transmitted), signal averaging would produce an invalid edge between the two real TP_IDL pulses. Averaging these two pulses would produce a signal that is not representative of either of the real TP_IDL pulses, so averaging is generally not a valid technique. The N5392A Ethernet compliance test application overcomes this problem by isolating the different TP_IDL pulses and averaging together only pulses of that width. This increases the amount of waveform captures required to make a pass/fail determination, but it greatly improves the measurement accuracy.

A user configurable number of waveforms are tested against the mask. The default number of waveforms tested is 100 for this test. The default number of averages is 512. The algorithm proceeds as described in the above section "Performing the Test".

NOTE The template requirements for this test are specified in such a way that testing with a digital oscilloscope is often impractical. Specifically, the large vertical and horizontal range of the masks will often result in failures when applying automated template test techniques. Specifically, you should exercise your own judgement when failures are marginal to determine if the signal shape is satisfactory.

NOTE Because the oscilloscope uses special triggering capabilities to qualify both variants of TP_IDL, this test can run slowly. One way to significantly speed up this test is to send very short packets so that the TP_IDL signal occurs frequently.

Measurements without TPM, Parametric Tests

Subclause 14.3.1.2 of IEEE 802.3-2008 defines the transmitter specifications a 10 Base-T Medium Access Unit (MAU) the MAU-to-MDI interface. Some of these tests require the use of an equivalent circuit that models the distortion of a simplex link segment. This is called the Twisted Pair Model (or TPM). There are also a number of tests that do not utilize the twisted pair model. To simplify test setup, tests performed without the TPM (section 6 of the test fixture, marked "10BT without TP Model") are organized in one section.

Jitter without TPM

This test ensures that the transmitter output jitter measured at the output of the twisted pair model (TPM), as defined in figure 14-18 of IEEE 802.3-2008, subclause 14.3.1.2.1, is within conformance limits. Jitter is measured with and without the TPM. This test measures jitter without the TPM. The jitter measurement is made with the TD circuit directly driving a 100 ohm resistive load.

References

[1] IEEE 802.3-2008, Subclause 14.3.1.2.3.

[2] IEEE 802.3-2008, Annex B.4.3.3.

[3] IEEE 802.3-2008, Annex B.4.1 "System Jitter budget".

Probing Setup

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

Refer to "Probing for 10 Base-T Tests Without the TPM, With Link Partner" on page 146.

1. Ensure that you short the appropriate load, as indicated in the connectivity instructions in the user interface.
2. Ensure the correct probe polarity.

Device Configuration

1. Reset the DUT if necessary
2. Configure the DUT to output 10 Base-T random data (see "Configuring a 10 Base-T Device to Output Random Data" on page 166).

3 Ensure that the oscilloscope is capturing proper signal (10 Base-T Random Data) as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel.
- Configure the oscilloscope to capture the 10 Base-T Random Data signal.
- Attempt, if Jitter Trigger Method is configured as “Automatic”, to determine the packet size and establish a stable trigger on a rising edge in the middle of the packet. If Jitter Trigger Method is configured as “Manual”, it will prompt you to configure the trigger system appropriately.
- Render the zero crossings at 8.0 BT or 8.5 BT, depending on the user selection for "10 Base-T Jitter Measurement" in the Configure tab.
- Continue to acquire and displaying waveforms until a user configurable number of jitter waveforms have been observed.
- Place a waveform histogram at the 0 V level, and measure the minimum and maximum deviation from the ideal edge location (8.0 BT or 8.5 BT).
- Ensure that the worst deviation is within conformance limits as listed in the Algorithm Discussion.

NOTE

If you have selected "ALL" as the "10 Base-T Jitter Measurement" (under the Configure tab), this test will be run at 8.0 BT and 8.5 BT. If you want to debug the 8.0 BT or 8.5 BT separately, select "Debug Mode" in the Configure tab, and select the individual test you wish to run. Note that for full compliance testing, you should test at both 8.0 BT and 8.5 BT as described in Reference[2]. At the result screen, 2 trials tabs are shown at the bottom left of the screen. Each trial tab shows the result of each test pair. For example, Trial 1 contains 8.0 BT result, Trial 2 contains 8.5 BT result and so on.

Algorithm Discussion

Reference [1] defines the integrated and external jitter specifications a 10 Base-T Medium Access Unit (MAU) at the MAU-to-MDI interface. This test does not use the twisted pair model (TPM). During the test the TPM is terminated in 100 ohms and driven by a transmitter with a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

In accordance with Annex B.4.3.3, An external MAU with a jitterless source driving DO is compliant when all zero crossings fall within the time ranges listed in Table 21. Two constraints are required: 8.0 bit time crossings and 8.5 bit time crossings. According to annex B.4.3.3 Note for 14.3.1.2.3 on output timing jitter, these two constraints completely determine compliance or noncompliance.

Table 21 Jitter Measurements* without TPM (cable)

MAU Type	Measurement	Limits
External	8.0 BT	8.0 BT +/- 16.0 ns
External	8.5 BT	8.5 BT +/- 16.0 ns
Internal	8.0 BT	8.0 BT +/- 20.0 ns
Internal	8.5 BT	8.5 BT +/- 20.0 ns

*The Jitter constraints are as per Reference[3].

A user configurable number of waveforms are acquired/analyzed for each measurement. The default number of waveforms is 10,000 for this test. You may wish to increase this number for more complete validation, or decrease it to speed up test time. The algorithm proceeds as described in the above section "Performing the Test".

Peak Differential Voltage

This test ensures that the peak differential output voltage on the TD circuit, as defined in Figure 14-8 of IEEE 802.3-2008, subclause 14.3.1.2.1, when terminated with a 100 ohm resistive load, is within conformance limits. This test does not utilize the twisted pair model. This measurement is made while the DUT is transmitting 10 Base-T Random Data.

References

[1] IEEE 802.3-2008, Subclause 14.3.1.2.1.

Probing Setup

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

Refer to "Probing for 10 Base-T Tests Without the TPM, With Link Partner" on page 146.

1. Ensure that you short the appropriate load, as indicated in the connectivity instructions in the user interface.
2. Ensure the correct probe polarity.

Device Configuration

1. Reset the DUT if necessary.
2. Configure the DUT to output 10 Base-T random data (see "Configuring a 10 Base-T Device to Output Random Data" on page 166).
3. Ensure that the oscilloscope is capturing proper signal (10 Base-T Random Data) as indicated in the connection instructions provided in the user interface.

Performing the Test

1. Ensure this test is checked to run in the "Select Tests" tab.
2. Press the "Run Tests" button in the task flow to start testing.
3. If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.
4. The test will:
   - Verify that the correct test signal is present on the configured "DUT Data" channel.
   - Configure the oscilloscope to capture the 10 Base-T Random Data signal, triggering on the rising edge of the data.
   - Capture 1000 positive pulses, measuring the peak voltage of each waveform. Record the minimum and maximum peak voltage of all positive pulses.
   - Configure the oscilloscope to capture the 10 Base-T Random Data signal, triggering on the falling edge of the data.

- Capture 1000 negative pulses, measuring the peak voltage of each waveform. Record the minimum and maximum peak voltage of all positive pulses.
- Ensure that the absolute value of the minimum and maximum of all peak voltages measured is between 2.2 and 2.8 V.

Algorithm Discussion

Reference [1] defines the differential output voltage specifications for a 10 Base-T Medium Access Unit (MAU) at the MAU-to-MDI interface. This test ensures that the peak differential output voltage on the TD circuit, as defined in Figure 14-8 of IEEE 802.3-2008, subclause 14.3.1.2.1, when terminated with a 100 ohm resistive load, is within conformance limits. This test does not utilize the twisted pair model. This measurement is made while the DUT is transmitting 10 Base-T Random Data.

The algorithm captures 1000 positive and 1000 negative pulses, measuring the peak voltage of each pulse. The minimum and maximum of both positive and negative pulses are recorded. For a compliant device, the worst case peak voltage measured must be between 2.2 and 2.8 V. The algorithm proceeds as described in the above section "Performing the Test".

Harmonic Content

This test ensures that the when the DO circuit is driven by all an ones Manchester encoded signal, any harmonic measured on the TD circuit, as defined in Figure 14-8 of IEEE 802.3-2008, subclause 14.3.1.2.1, is at least 27 dB below the fundamental. This test does not utilize the twisted pair model. This measurement is made while the DUT is transmitting an all ones Manchester-encoded signal (1010101010...).

References

[1] IEEE 802.3-2008, Subclause 14.3.1.2.1.

Probing Setup

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

Refer to "Probing for 10 Base-T Tests Without the TPM, With Link Partner" on page 146.

1. Ensure that you short the appropriate load, as indicated in the connectivity instructions in the user interface.
2. Ensure the correct probe polarity.

Device Configuration

1 Reset the DUT if necessary.

2 Configure the DUT to output 10 Base-T Manchester Encoded harmonic ones data (see "Configuring a 10 Base-T Device to Output Manchester Encoded Harmonic Ones" on page 167).

NOTE

An alternate method, allowed by reference [1], is to configure the DUT to send maximum length packets with a payload of all ones.

3 Ensure that the oscilloscope is capturing proper signal (10 Base-T Manchester Encoded harmonic ones) as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "DUT Data" channel.
- Configure the oscilloscope to capture the 10 Base-T all ones Manchester Encoded signal.
- Capture 100 microseconds of data.
- Perform a FFT on the data to measure spectral power.
- Measure the power at the fundamental (10 MHz).
- Measure the power at each harmonic that has at a peak level of at least -40 dB.
- Ensure that each harmonic is at least 27 dB down from the fundamental.

Algorithm Discussion

Reference [1] defines the harmonic content specifications for a 10 Base-T Medium Access Unit (MAU) at the MAU-to-MDI interface. This test ensures that the when the DO circuit is driven by all an ones Manchester encoded signal, any harmonic measured on the TD circuit, as defined in Figure 14-8 of IEEE 802.3-2008, subclause 14.3.1.2.1, is at least 27 dB below the

fundamental. This test does not utilize the twisted pair model. This measurement is made while the DUT is transmitting an all ones Manchester-encoded signal (1010101010...).

This test captures 100 microseconds of alternating 10101010 data, and computes an FFT of the data signal. The algorithm proceeds as described in the above section "Performing the Test".

Common Mode Voltage Tests

Common Mode Output Voltage

This test ensures that magnitude of the total common-mode output voltage of the transmitter, Ecm, measured as shown in Figure 14-14 of IEEE 802.3-2008, subclause 14.3.1.2.7 is less than 50 mV peak. Common Mode voltage is measured over a period of time and the peak-to-peak common mode output voltage is measured as the largest absolute value of the worst case minimum or worst case maximum common mode output voltage.

References

[1] IEEE 802.3-2008, Subclause 14.3.1.2.7.

Probing Setup

NOTE

Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

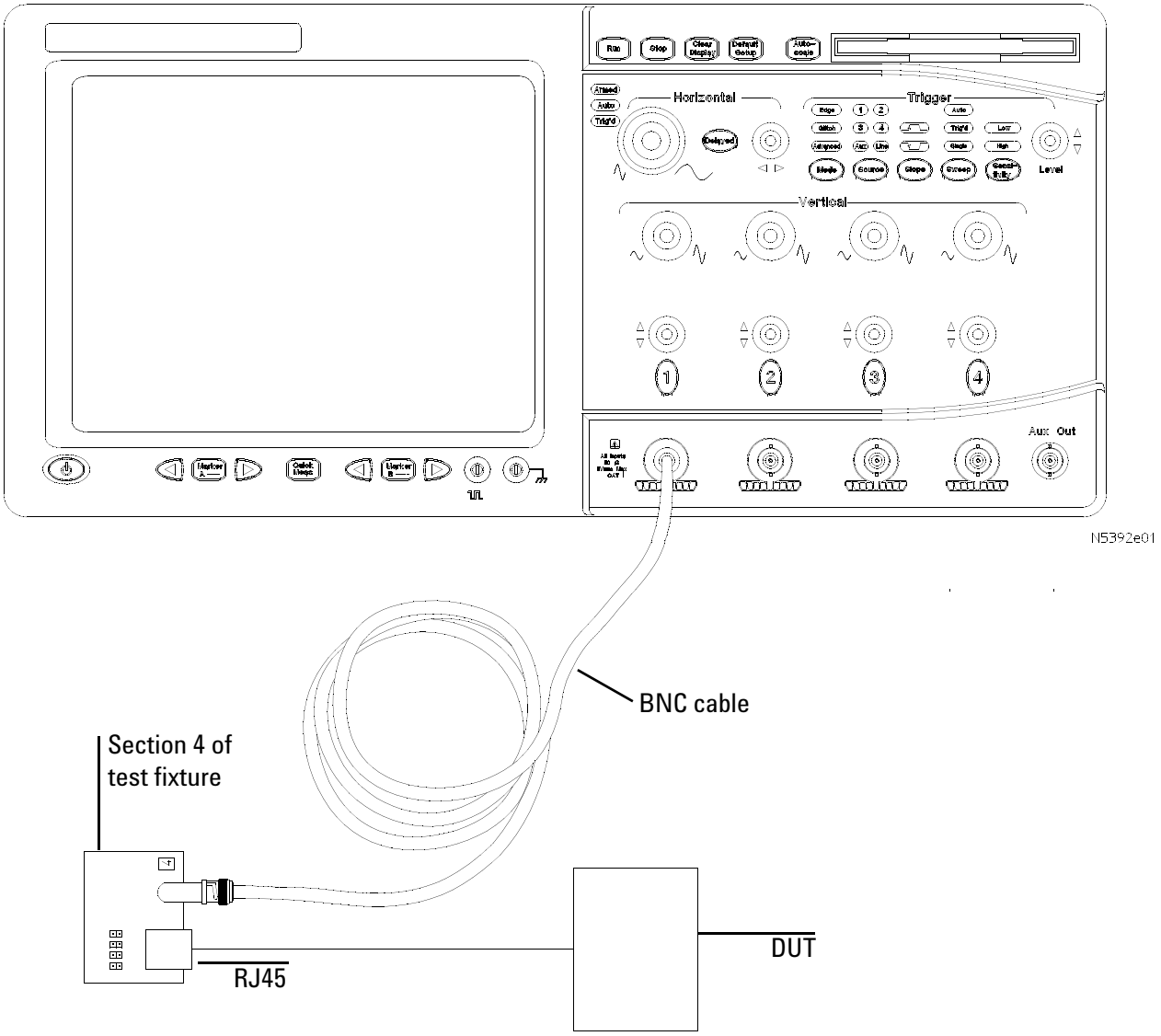


Figure 37 Probing for 10 Base-T Common Mode Output Voltage

1 Connect the DUT to the RJ45 connector on fixture 4 using a short UTP cable.

2 Using a single jumper, short the appropriate pins for pair A on fixture 4.

3 Using a short BNC cable, connect the BNC connector on fixture 4 to the configured “Common Mode” channel on the oscilloscope.

Device Configuration

1 Configure the DUT to output 10 Base-T Random Data. Contact your PHY vendor for instructions on configuring the DUT to transmit 10 Base-T Random data without a link partner.

2 Ensure that the DUT is transmitting the proper signal as indicated in the connection instructions provided in the user interface.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will:

- Verify that the correct test signal is present on the configured "Common Mode" channel.
- Capture multiple acquisitions totaling 100 ms of the common mode output voltage signal Ecm_out as indicated in figure 14-14 of Reference [1]. Display this signal as a color-graded persistence waveform.
- Record the worst case minimum and maximum voltage encountered over all acquired data.
- Compute the worst case peak common mode output voltage as the maximum absolute value of the worst case maximum and worst case minimum voltage.

Algorithm Discussion

Reference [1] defines the maximum common mode output voltage specifications for a 10 Base-T Medium Access Unit (MAU) at the MAU-to-MDI interface. This test ensures that magnitude of the total common-mode output voltage of the transmitter, Ecm, measured as shown in Figure 14-14 of IEEE 802.3-2008, subclause 14.3.1.2.7 is less than 50 mV peak. This test does not utilize the twisted pair model. This measurement is made while the DUT is transmitting 10 Base-T Random Data.

The total Common Mode voltage Ecm_out is measured over a 100 ms duration and the peak common mode output voltage is computed as the largest absolute value of the worst case minimum and worst case maximum common mode output voltage.

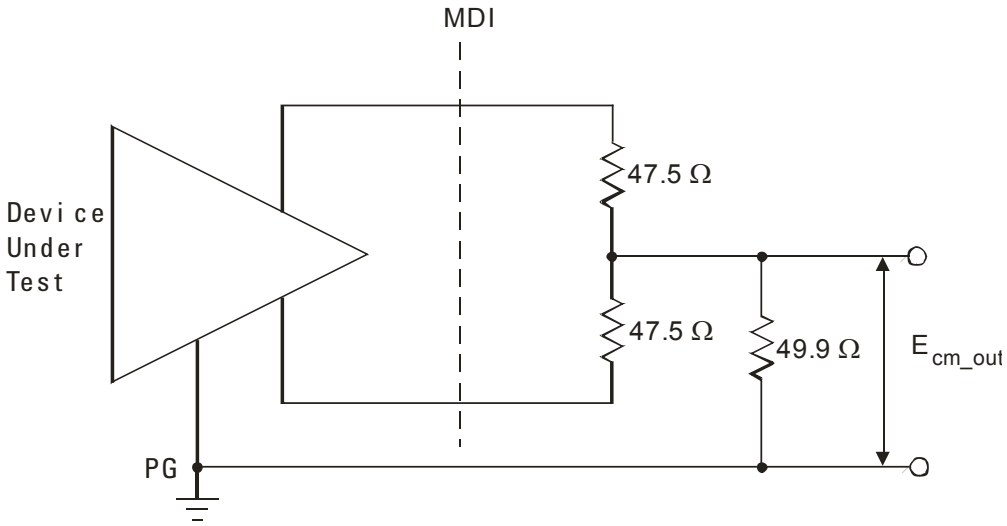


Figure 38 Common Mode Output Voltage Test Circuit

Configuring 10 Base-T Device Output

Configuring a 10 Base-T Device to Output Random Data

A random data signal is required for some 10 Base-T tests. This section provides some commonly used methods to configure a DUT to output random data.

NOTE Special boot software and/or a link partner may be required to obtain 10 Base-T Random data. Contact your PHY vendor for boot software or specific instructions on configuring the DUT to output random data.

- If you have a 10 Base-T link-partner transmitting idle pulses, connect the link partner to the same fixture using the RJ45 port marked “LP”.
- You may also be able to configure the DUT to output 10 Base-T random data using special boot software (in some cases a link partner is still required).
- If custom boot software is available, the PHY vendor should provide instructions. However, you may be able to configure the DUT to output Random data with some combination of the following steps:
  - Disable link speed negotiation.
  - Force the link-speed to 10-BASE-T.
  - Configure the device to transmit data.
  - In most cases, with special boot software, you can control the output data. Configure the output data as “random”.
  - If no custom boot software is available, you may be able to use high-level software programs like “ipsend” (UNIX) or “pktsend” (DOS) to specify the packet payload.

NOTE If you are performing MAU Template or Jitter tests, the DUT should be configured to output packets of random data of sufficient length. The data must be random in order to capture all possible data sequences. A minimum packet length of 300 bytes is recommended for the Automatic Jitter Trigger method.

Configuring a 10 Base-T Device to Output Manchester Encoded Harmonic Ones

A Manchester encoded all ones signal (0101010...) is required for the 10 Base-T Harmonic Test. This section provides some commonly used methods to configure a DUT to output this signal.

NOTE Special boot software and/or a link partner may be required to obtain 10 Base-T Harmonic Ones signal. Contact your PHY vendor for boot software or specific instructions on configuring the DUT to output this signal.

- If you have a 10 Base-T link-partner, you may need to connect the link partner to the same fixture using the RJ45 port marked “LP”.
- You may also be able to configure the DUT to output 10 Base-T Harmonic Ones signal using special boot software (in some cases a link partner is still required).
- If custom boot software is available, the PHY vendor should provide instructions. However, you may be able to configure the DUT to output the appropriate signal with some combination of the following steps:
  - Disable link speed negotiation.
  - Force the link-speed to 10-BASE-T.
  - Configure the device to transmit data.
  - In most cases, with special boot software, you can control the output data. Configure the output data as all FF or all ones (remember that the signal is Manchester Encoded, so 11111 is encoded as 101010 on the wire.
  - If no custom boot software is available, you may be able to use high-level software programs like “ipsend” (UNIX) or “pktsend” (DOS) to specify the packet payload.

Transmitter Return Loss

NOTE This section shows the use of a Vector Network Analyzer (VNA) used for testing Transmitter Return Loss. However, you can use in place of the VNA an exported VNA file in either the Touchstore or CITI file format.

This section describes the 10 Base-T Transmitter Return Loss test as per IEEE802.3-2008, Subclause 14.3.1.2.2 and Annex B.4.3.2. The test procedures described in this section cover the Transmitter Return Loss measurement required by the specification.

Reference

[1] IEEE802.3-2008, Subclause 14.3.1.2.2 and Annex B.4.3.2.

Calibrating the VNA

Before using the VNA, it must be calibrated using the Return Loss Calibration board. See Figure 39 for the connection diagram.

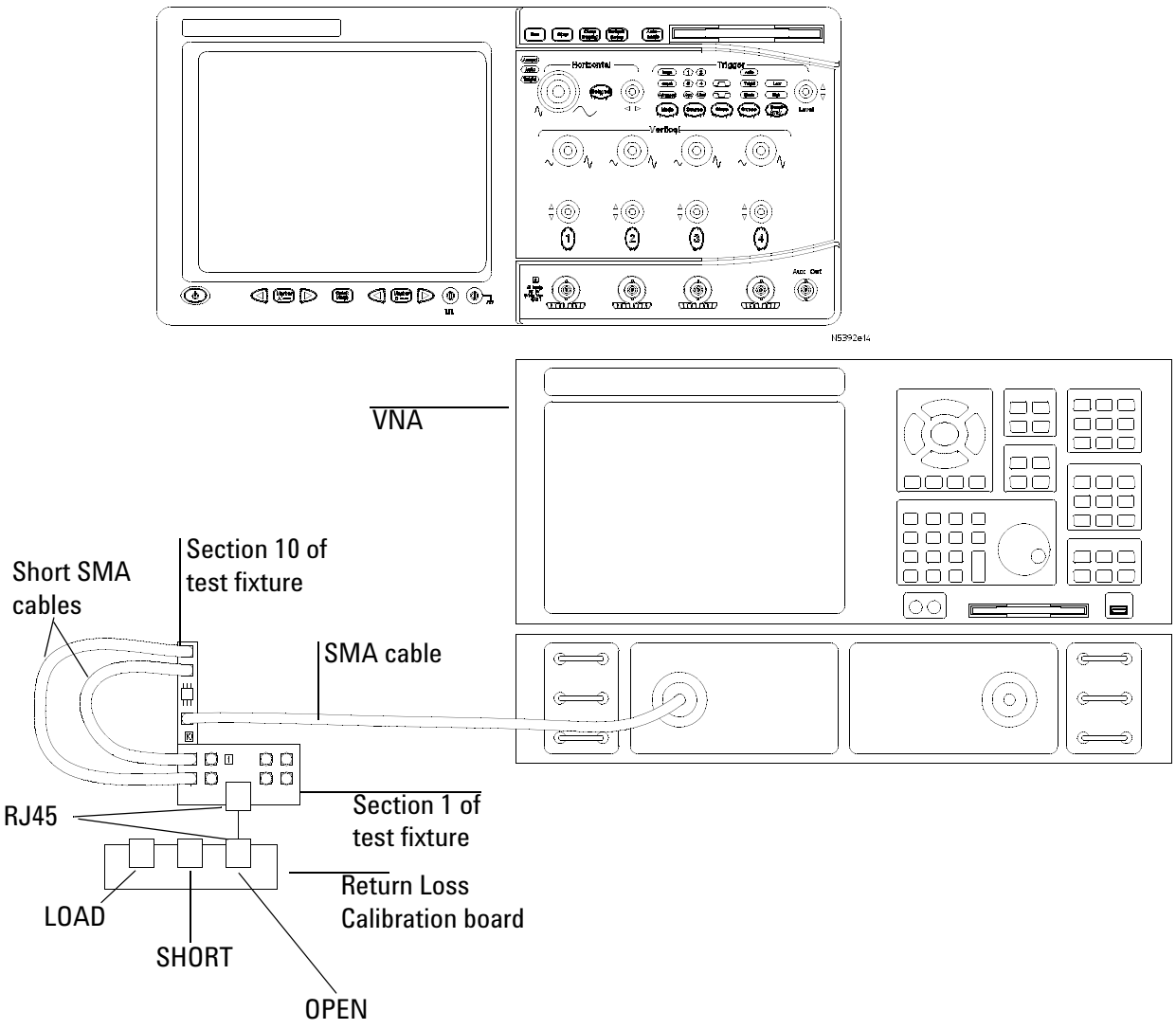


Figure 39 VNA Calibration

1 Connect the Return Loss Calibration board RJ45 connector labeled OPEN to the RJ45 connector on fixture 1 using a short straight-through UTP cable.

2 Connect one end of two short SMA-to-SMA cables to the SMA test points for the pair A you are testing on fixture 1, and the other end to the two SMA (X97 and X98) test points on fixture 10.

3 Connect a VNA input to the SMA (X99) test point on fixture 10.

4 Calibrate the VNA using the instructions in the VNA's User's Guide. The following is a list of setup requirements.
   - Set Meas to Ref1 Fwd S11.
   - Set Start to 5.0 MHz.
   - Set Stop to 10 MHz.
   - Set Format to Log Mag.
   - Set Scale Div to 5.
   - Set Scale Ref to reference line position 9.
5 Run the calibration for the OPEN, SHORT, and LOAD connections.

Probing Setup for Transmitter Return Loss

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

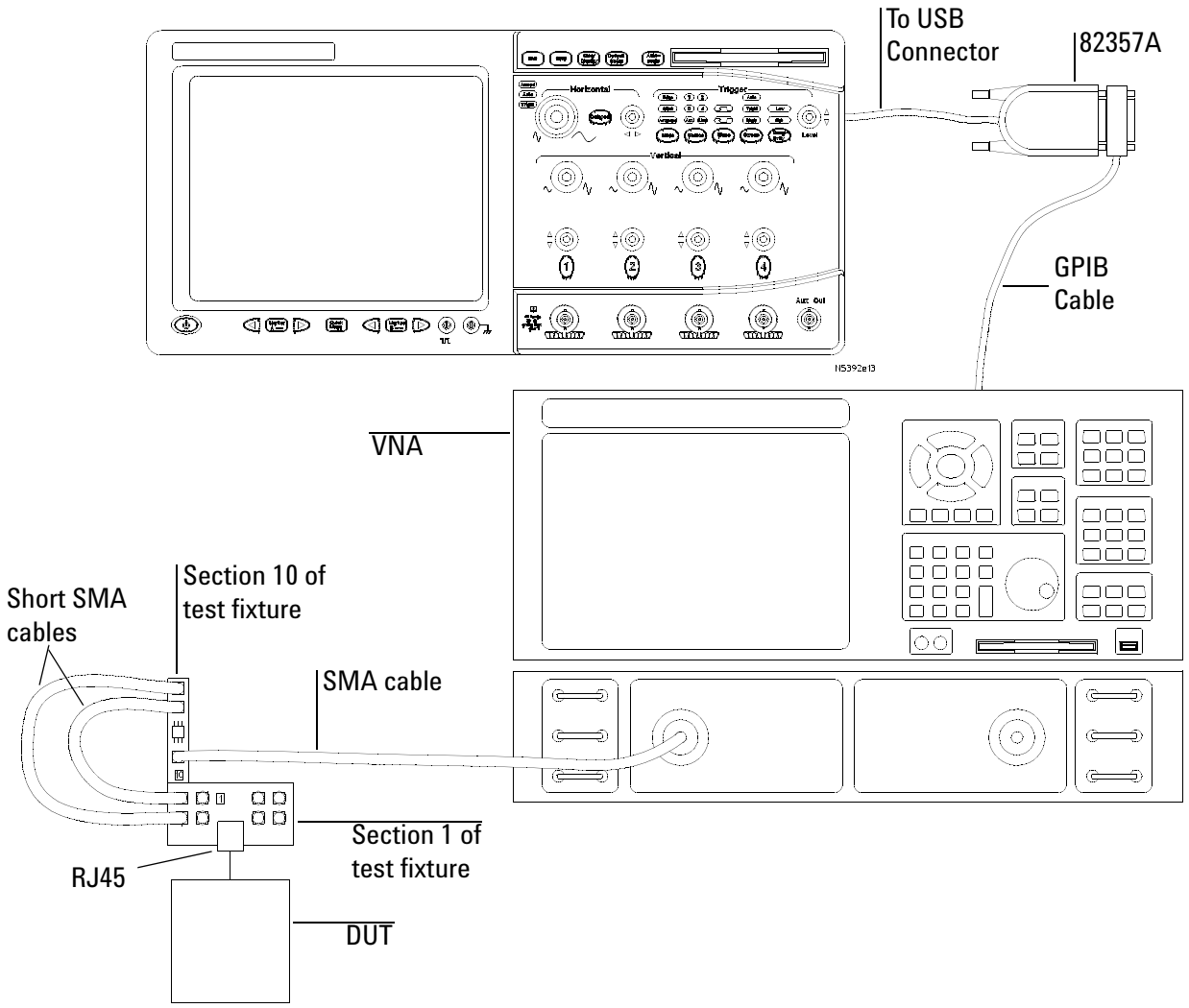


Figure 40 Probing for 10 Base-T Transmitter Return Loss

1. Connect the DUT to the RJ45 connector on fixture 1 using a short straight-through UTP cable.
2. Connect one end of two short SMA-to-SMA cables to the SMA test points for testing the pair A on fixture 1, and the other end to the two SMA (X97 and X98) test points on fixture 10.
3. Connect a VNA input to the SMA (X99) test point on fixture 10.

4 Connect a GPIB cable to the 82357A GPIB port and to the GPIB port on the VNA.

5 Connect the 82357A USB connector to a USB port on the scope.

Device Configuration

1 Configure the DUT to output 10Base-T random data.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will compute the return loss as described in the Algorithm Discussion below.

Algorithm Discussion

Reference [1] describes all the receive channel return loss specifications for a 10 Base-T device at the physical medium attachment (PMA). The differential output impedance as measured on the TD circuit shall be such that any reflection, due to differential signals incident upon the TD circuit from a simplex link segment having any impedance within the range specified in 14.4.2.2, shall be at least 15 dB below the incident, over the frequency range of 5.0 MHz to 10 MHz. This return loss shall be maintained at all times when the MAU is powered, including when the TD circuit is sending TP_IDL.

Receiver Return Loss

NOTE This section shows the use of a Vector Network Analyzer (VNA) used for testing Receiver Return Loss. However, you can use in place of the VNA an exported VNA file in either the Touchstore or CITI file format.

This section describes the 10 Base-T Receiver Return Loss test as per IEEE 802.3-2008, Subclause 14.3.1.3.4 and Anex B.4.3.5. The test procedures described in this section cover the Receiver Return Loss measurement required by the specification.

Reference

[1] IEEE 802.3-2008, Subclause 14.3.1.3.4 and Anex B.4.3.5

Calibrating the VNA

Before using the VNA, it must be calibrated using the Return Loss Calibration board. See Figure 41 for the connection diagram.

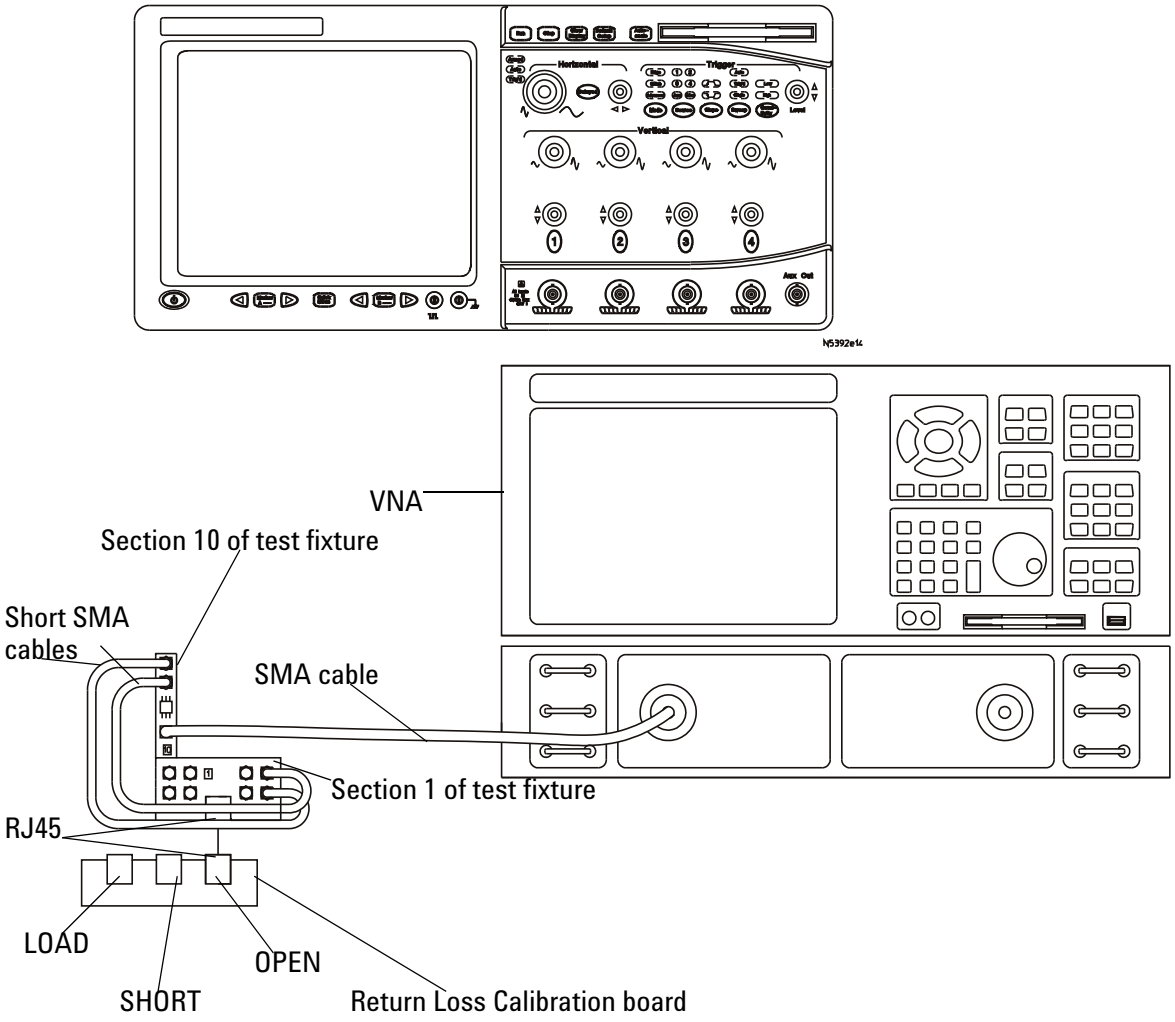


Figure 41 VNA Calibration

1 Connect the Return Loss Calibration board RJ45 connector labeled OPEN to the RJ45 connector on fixture 1 using a short straight-through UTP cable.

2 Connect one end of two short SMA-to-SMA cables to the SMA test points for the pair B you are testing on fixture 1, and the other end to the two SMA (X97 and X98) test points on fixture 10.

3 Connect a VNA input to the SMA (X99) test point on fixture 10.

4 Calibrate the VNA using the instructions in the VNA's User's Guide. The following is a list of setup requirements.

- Set Meas to Ref1 Fwd S11.
- Set Start to 5.0 MHz.
- Set Stop to 10 MHz.
- Set Format to Log Mag.
- Set Scale Div to 5.
- Set Scale Ref to reference line position 9.

5 Run the calibration for the OPEN, SHORT, and LOAD connections.

Probing Setup for Receiver Return Loss

NOTE Before starting a test, you can view these connection instructions under the application's Connect tab. If connection changes are necessary while tests are running, the application automatically prompts you with new connection instructions.

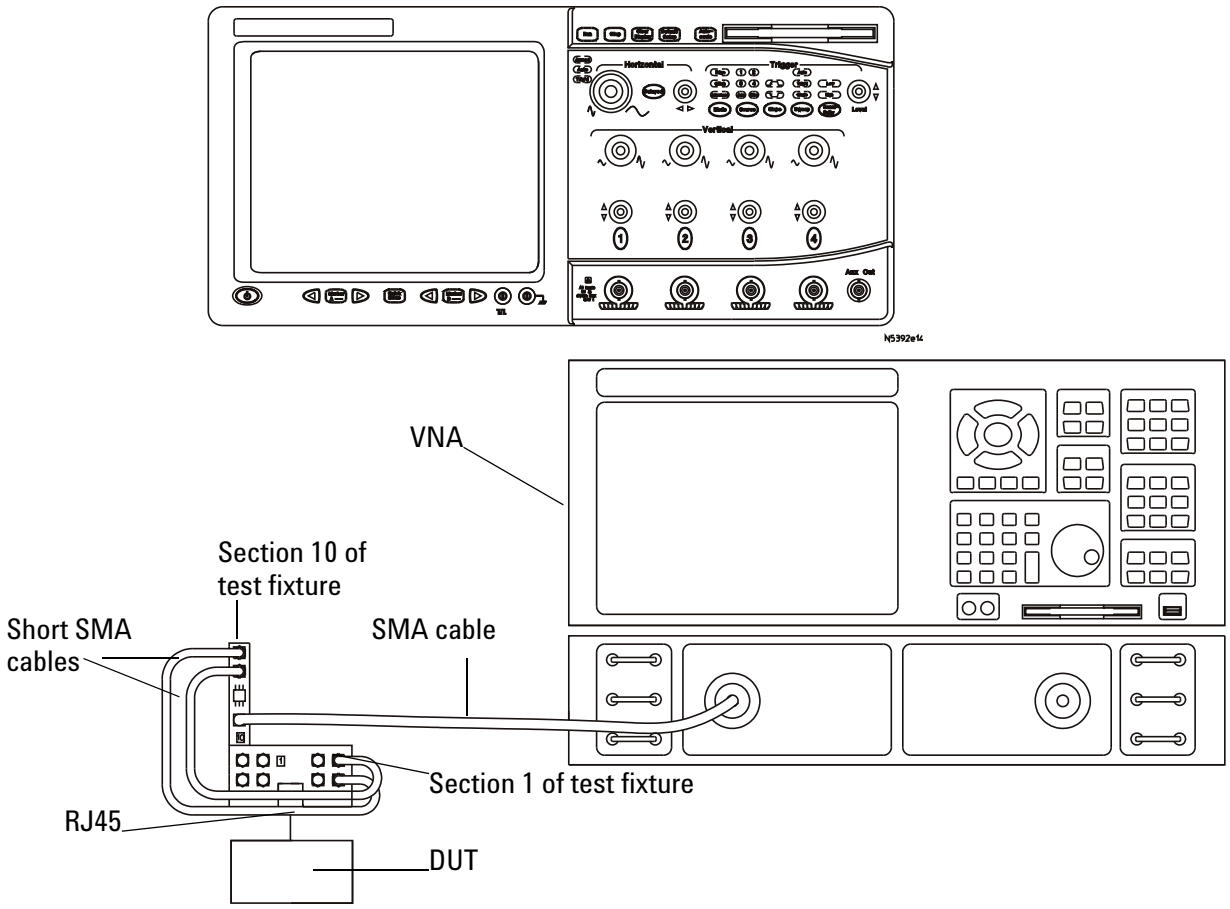


Figure 42 Probing for 10 Base-T Receiver Return Loss

1 Connect the DUT to the RJ45 connector on fixture 1 using a short straight-through UTP cable.

2 Connect one end of two short SMA-to-SMA cables to the SMA test points for testing the pair B on fixture 1, and the other end to the two SMA (X97 and X98) test points on fixture 10.

3 Connect a VNA input to the SMA (X99) test point on fixture 10.

4 Connect a GPIB cable to the 82357A GPIB port and to the GPIB port on the VNA.

5 Connect the 82357A USB connector to a USB port on the scope.

Device Configuration

1 The DUT for 10 Base-T operation does not require any particular configuration. Simply turn on the DUT and set the DUT to operate in 10 Base-T to perform the test.

Performing the Test

1 Ensure this test is checked to run in the "Select Tests" tab.

2 Press the "Run Tests" button in the task flow to start testing.

3 If the system is not physically configured to perform this test, the application will prompt you to change the physical configuration. When you have completed these instructions, check the box next to "I have completed these instructions" near the bottom of this dialog. Then, press the "Next" button to continue testing.

4 The test will compute the return loss as described in the Algorithm Discussion below.

Algorithm Discussion

Reference [1] describes all the receive channel return loss specifications for a 10 Base-T device at the physical medium attachment (PMA). The differential input impedance shall be such that any reflection, due to differential signals incident upon the RD circuit from a twisted pair having any impedance within the range specified in 14.4.2.2, shall be at least 15 dB below the incident, over the frequency range of 5.0 MHz to 10 MHz. This return loss shall be maintained at all times when the MAU is powered.

7 Calibrating the Infiniium Oscilloscope and Probe

This appendix describes the Agilent Infiniium digital storage oscilloscope calibration procedures.

Required Equipment for Calibration

To calibrate the Infiniium oscilloscope in preparation for running the Ethernet automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2, (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the 54850A series, 80000 and 90000A series Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable.
- BNC shorting cap (provided with the Agilent Infiniium oscilloscope).

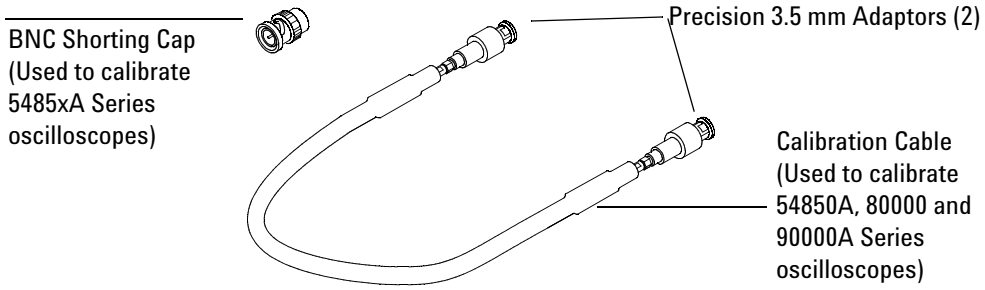


Figure 43 Accessories Provided with the Agilent Infiniium Oscilloscope

Internal Calibration

To perform an internal diagnostic and calibration cycle for the oscilloscope (referred as Calibration for the Agilent oscilloscope), follow these steps:

1 Set up the oscilloscope with the following steps:

   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.

   b Plug in the power cord.

   c Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.

   d Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:

   a Locate the BNC shorting cap.

   b Locate the calibration cable.

   c Locate the two Agilent precision SMA/BNC adapters.

   d Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.

   e Attach another SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 44 below, perform the following steps:

a Click on the Utilities>Calibration menu to open the Calibration dialog box.

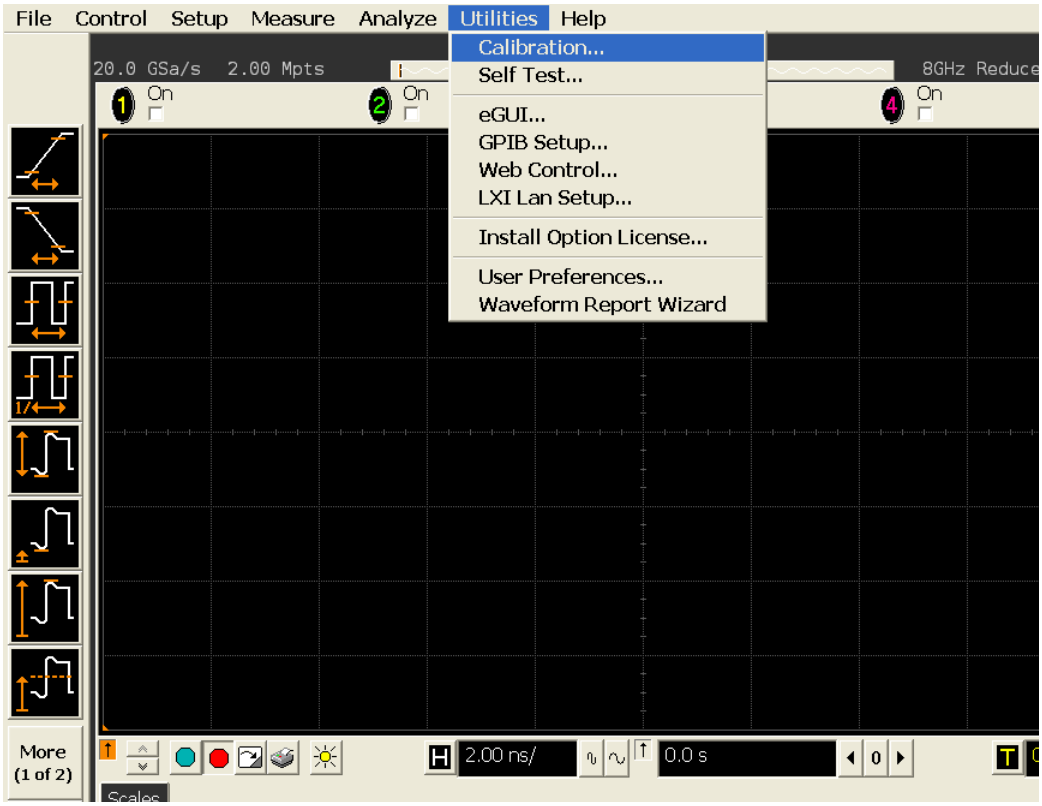


Figure 44 Accessing the Calibration Menu.

4 Referring to Figure 45 below, perform the following steps to start the calibration:

b Uncheck the Cal Memory Protect checkbox.

c Click the Start button to begin the calibration.

d Follow the on-screen instructions.

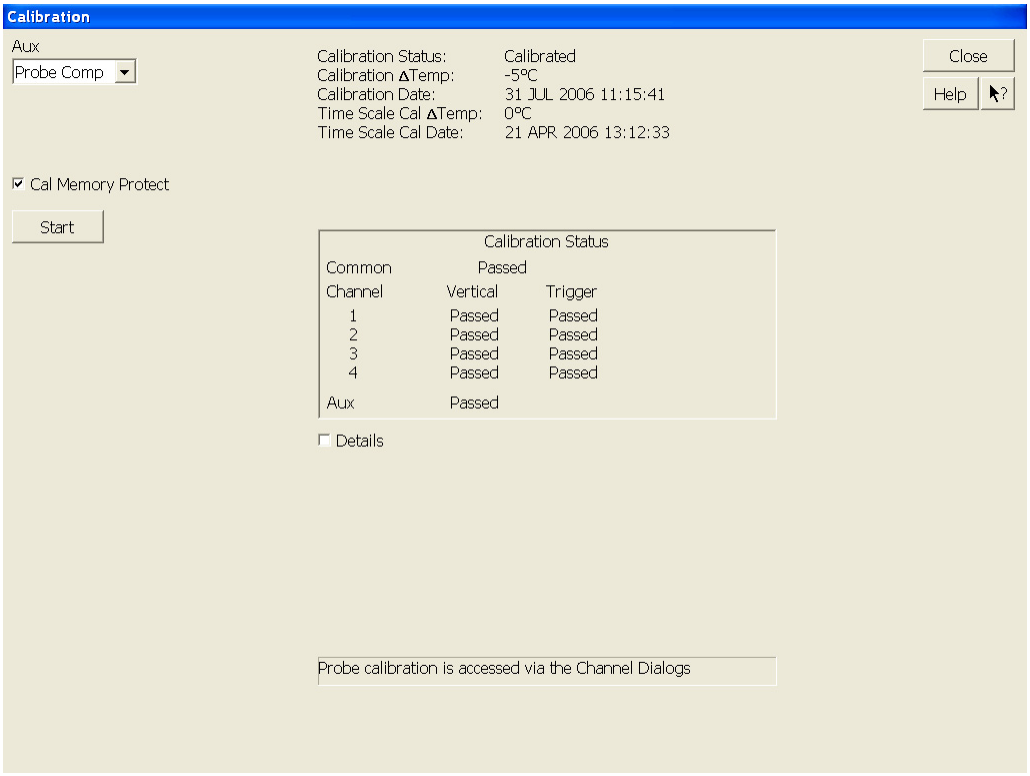


Figure 45 Oscilloscope Calibration Window

e During the calibration of channel 1, if you are prompted to perform a Time Scale Calibration, as shown in Figure 46 below.

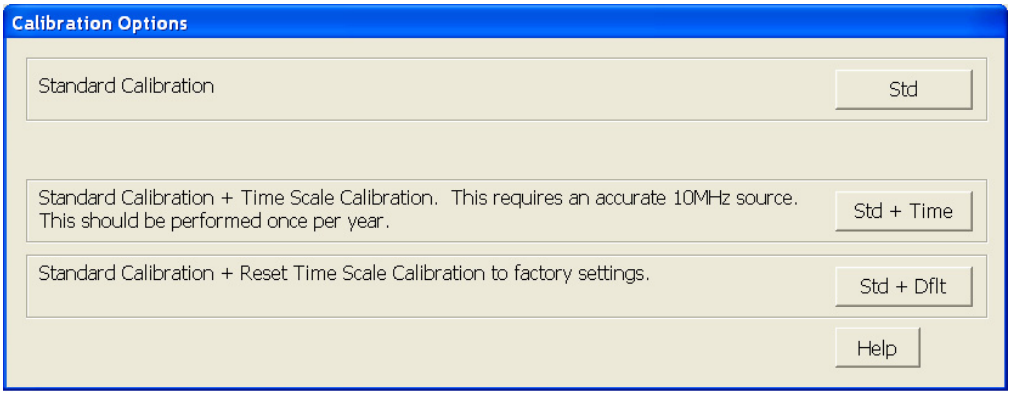


Figure 46 Time Scale Calibration Dialog box

f Click on the Default button to continue the calibration, using the Factory default calibration factors.

g When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

h Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

i Click the Close button to close the calibration window.

j The internal calibration is completed.

k Read NOTE below.

NOTE These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Probe Calibration

Before performing Ethernet tests you should calibrate the probes.

Probe Atten/Offset Calibration

This procedure shows the differential socketed probe head calibration as an example. This procedure should be used to calibrate all of the addition probe heads used for the Ethernet tests.

1 Referring to Figure 47 below, perform the following steps:

a If you are calibrating the differential socketed probe head, install the 82 Ω resistors into the ends of the sockets. These resistors are only required for probe calibration.

b Click on the Setup>Channel 1 menu to open the Channel Setup window.

Figure 47 Channel Setup Window.

c Click the Probes button in the Channel Setup window, to open the Probe Setup window.

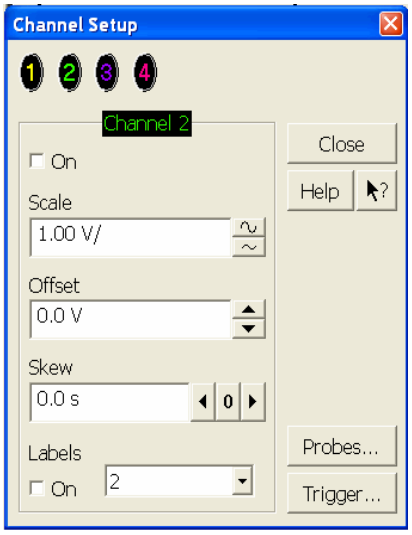


Figure 48 Channel Dialog Box

2 Referring to Figure 49 below, perform the following steps:

a Click the Add Head... button, and then select E2678A:DF Sckt from the list of Head Type. Select OK to close the dialog box.

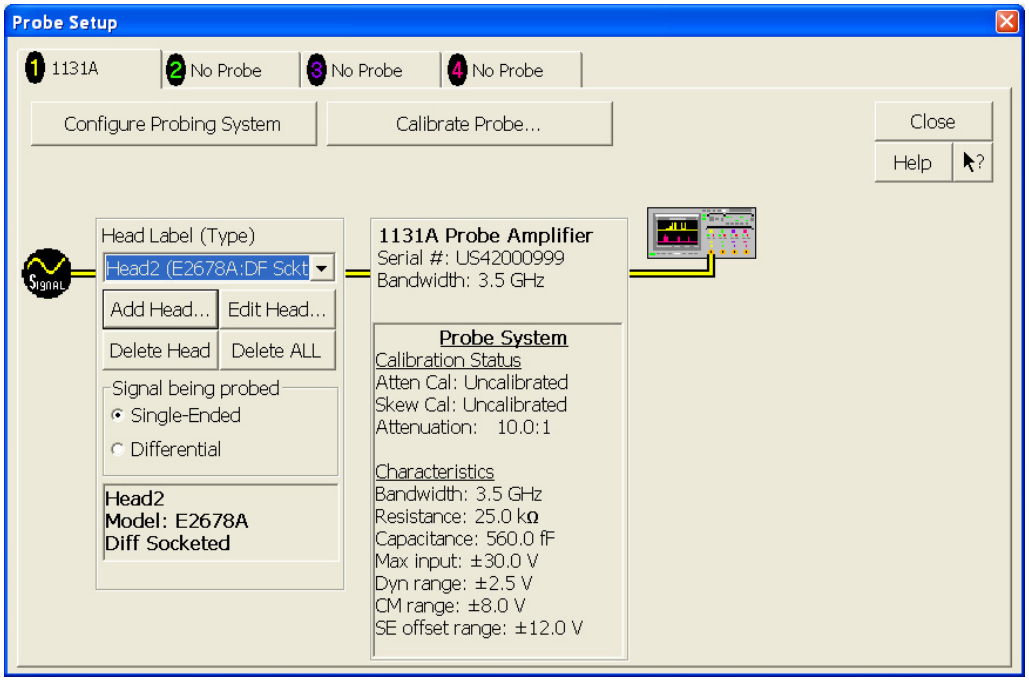


Figure 49 Probe Setup Window.

3 Referring to Figure 50 below, perform the following steps:

a Click on the Calibrate Probe button to open the Probe Calibration window.

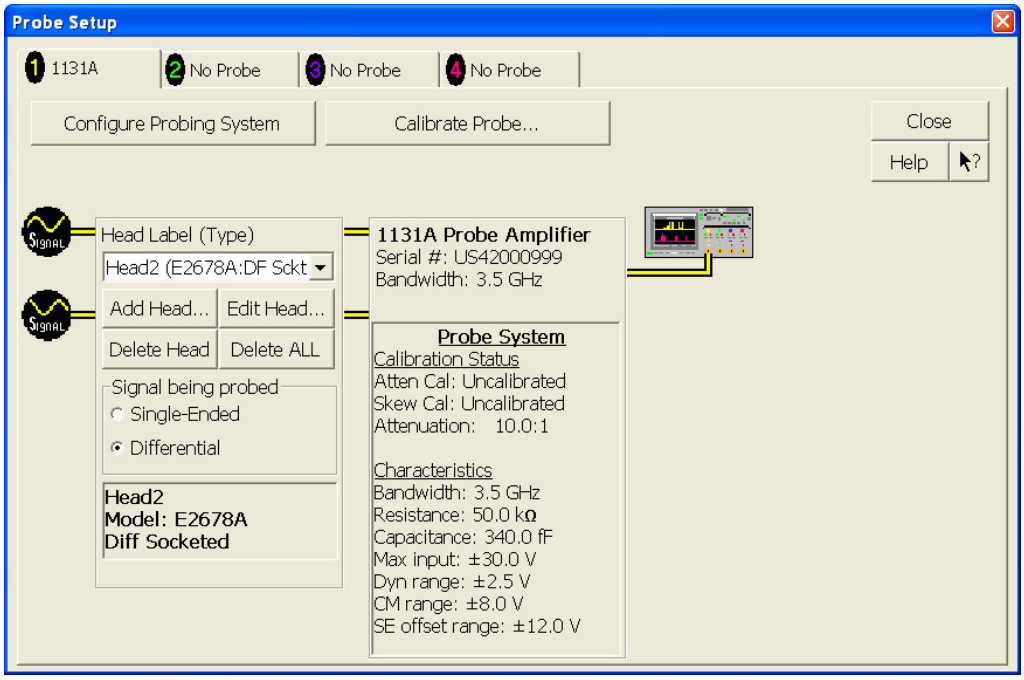


Figure 50 Calibrating a Probe.

4 Referring to Figure 51 below, perform the following steps:

a Select the Calibrated Atten/Offset Radio Button

b Click the Start Atten/Offset Calibration Button to open the Calibration window.

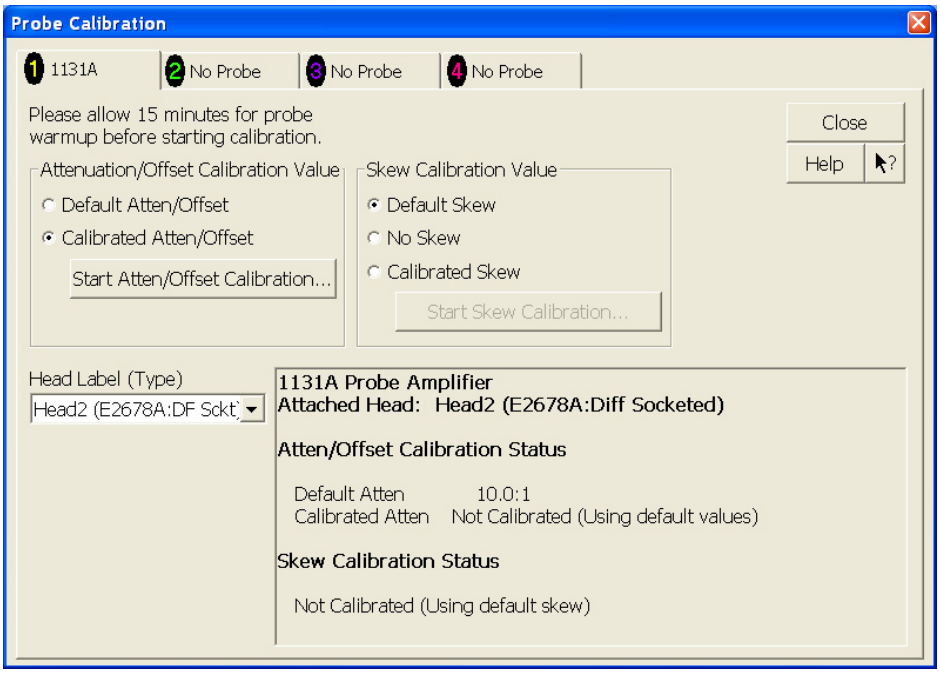


Figure 51 Probe Calibration Window.

c Follow the on screen instructions.

5 At the end of each calibration, the oscilloscope will prompt you if the calibration was or was not successful.

8 InfiniiMax Probing

Agilent recommends the E2678A differential socket probe head and E2677A solder-in differential probe head. All InfiniiMax active differential probes can be used with the N5392A Ethernet Compliance Test Application.

Figure 52 Recommended Probe Head for the Ethernet Compliance Test Application

Table 22 Probe Head Characteristics

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential socketed	E2678A	7 GHz, 0.34 pF, 50 kW	7 GHz, 0.56 pF, 25 kW
Differential solder-in	E2677A	12 GHz, 0.27 pF, 50 kW	12 GHz, 0.44 pF, 25 kW

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